利用Quartus-II进行仿真实验

原创

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目录

> 实验目的：
> 1.在 Quartus-II 中自己用门电路设计一个D触发器，并进行仿真，时序波形验证。
> 2.在 Quartus-II 中直接调用一个D触发器电路，进行仿真，时序波形验证，与1做比较；
> 3.在 Quartus-II用Verilog语言写一个D触发器，进行仿真验证，与2做比较；
> 实验环境：Quartus-II安装
> 参考资料：使用

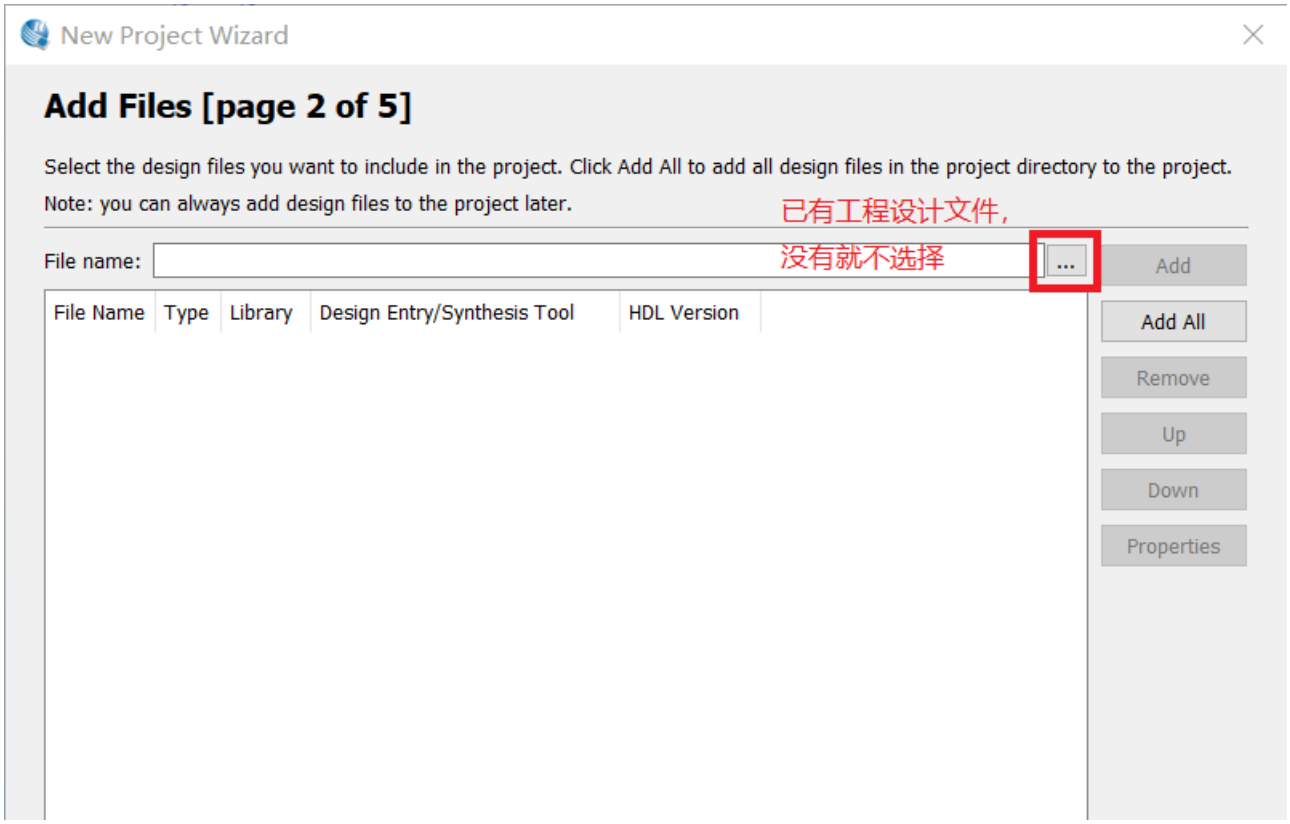
一、设计D触发器

1.新建工程

找到File——》new project W…——》next

然后进行以下操作，其余全是next

这里不用选，直接next



Specify the path names of any non-default libraries. User Libraries...

< Back | Next > | Finish | Cancel | Help

New Project Wizard

Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

Device family

选择芯片系列

Family: Cyclone IV E

Devices: All

Target device

- Auto device selected by the Fitter
- Specific device selected in 'Available devices' list
- Other: n/a

Show in 'Available devices' list

Package: Any

Pin count: Any

Speed grade: Any

Name filter: EP4CE115F29C7

Show advanced devices

搜索芯片

Available devices:

Name	Core Voltage	LEs	User I/Os	Memory Bits	Embedded multiplier 9-bit element
EP4CE115F29C7	1.2V	114480	529	3981312	532

选择芯片

< Back | Next > | Finish | Cancel | Help

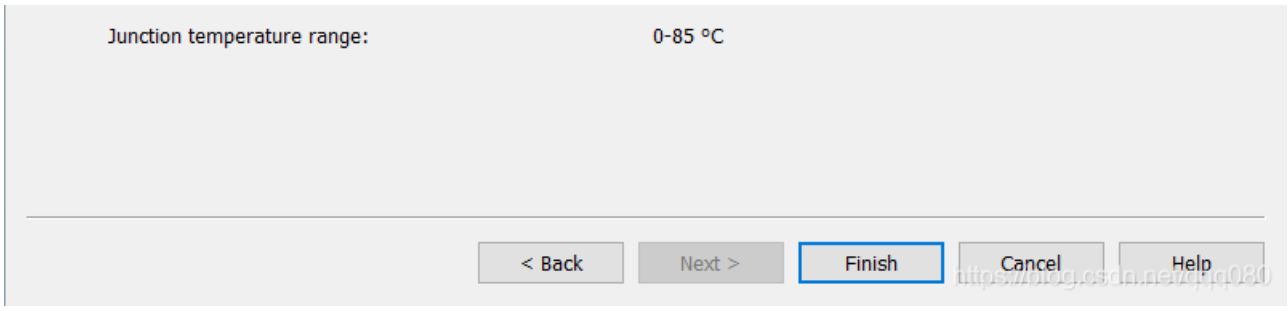
New Project Wizard

Summary [page 5 of 5]

创建的工程信息

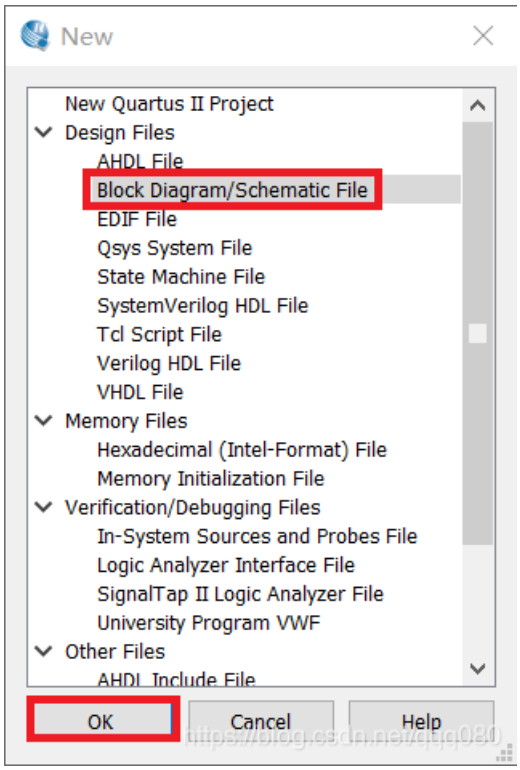
When you click Finish, the project will be created with the following settings:

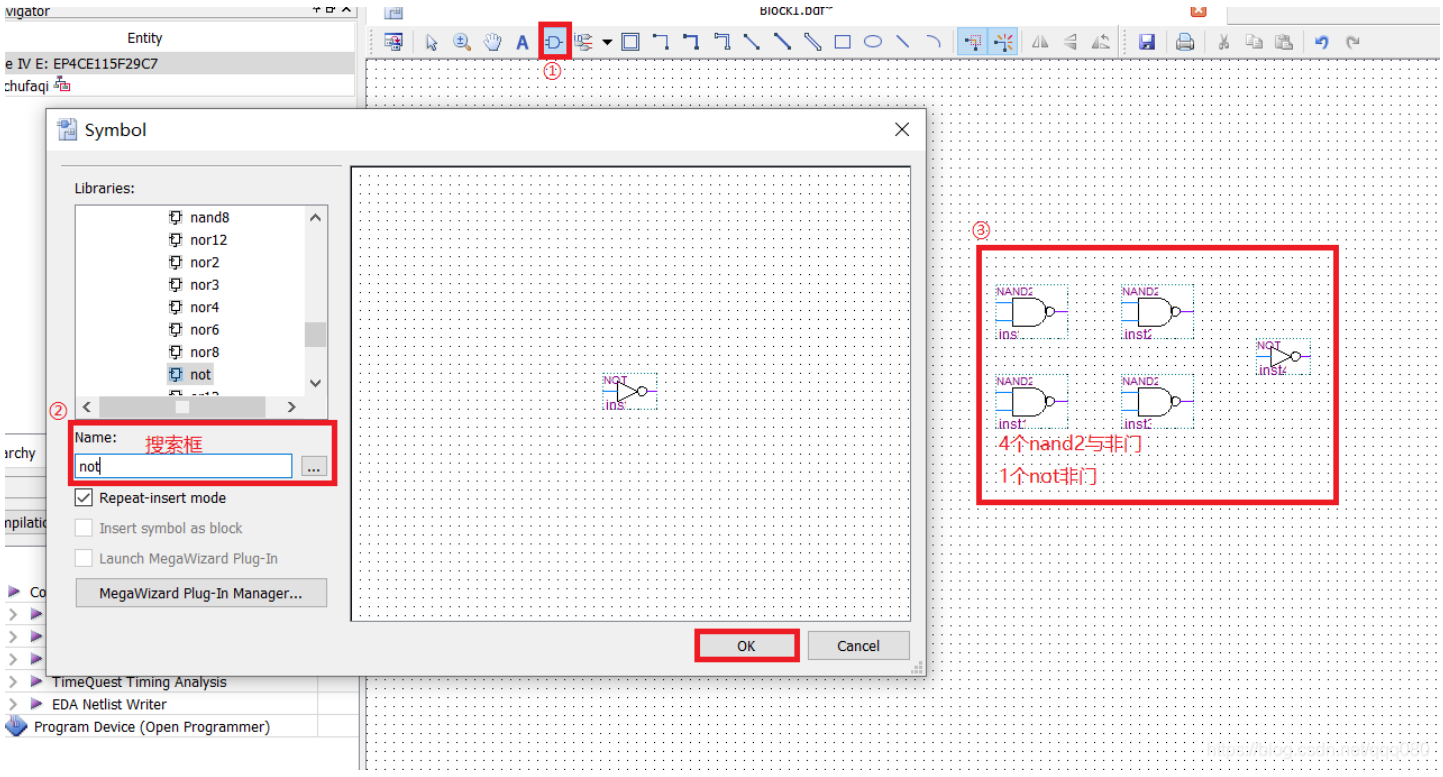
Project directory:	E:/01work_area/IOT_homework2/qrs4/Q1
Project name:	D_chufaqi
Top-level design entity:	D_chufaqi
Number of files added:	0
Number of user libraries added:	0
Device assignments:	
Family name:	Cyclone IV E
Device:	EP4CE115F29C7
EDA tools:	
Design entry/synthesis:	<None> (<None>)
Simulation:	<None> (<None>)
Timing analysis:	()
Operating conditions:	
VCCINT voltage:	1.2V

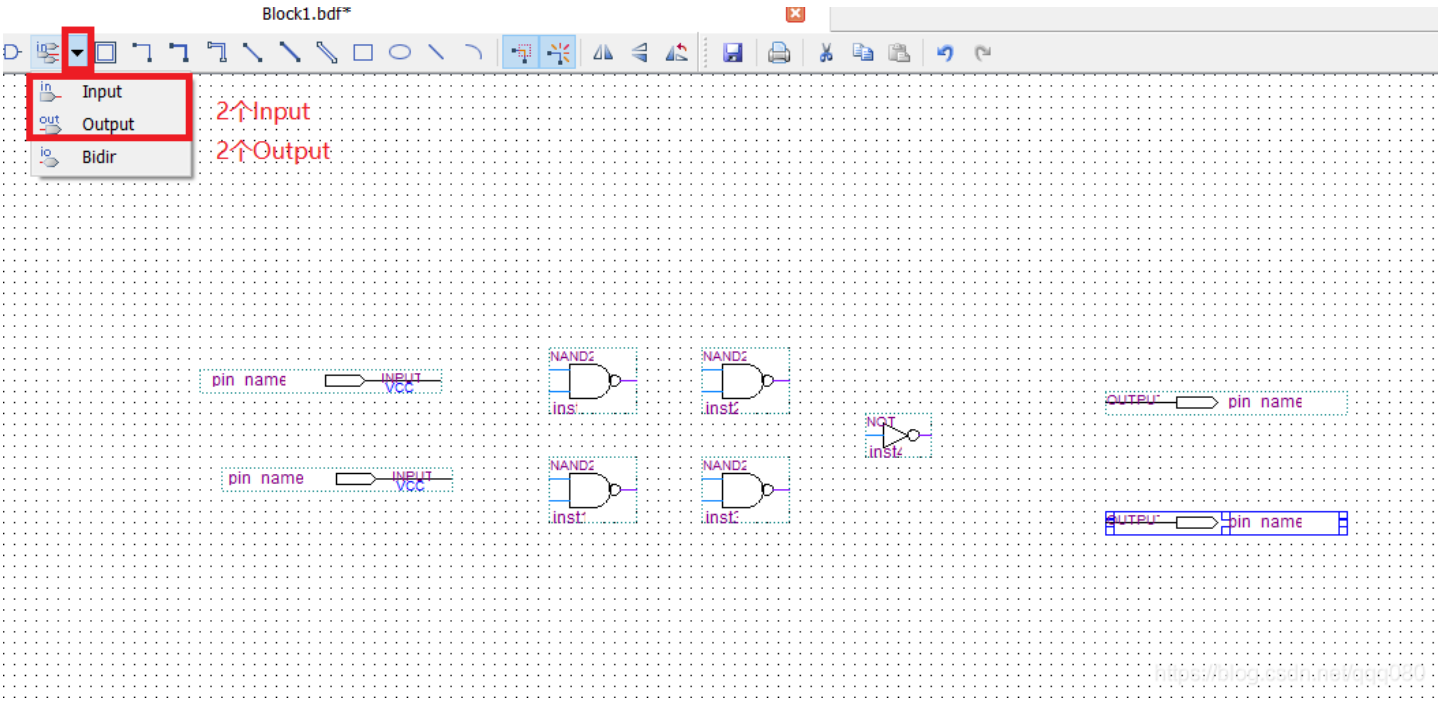


2.创建原理图

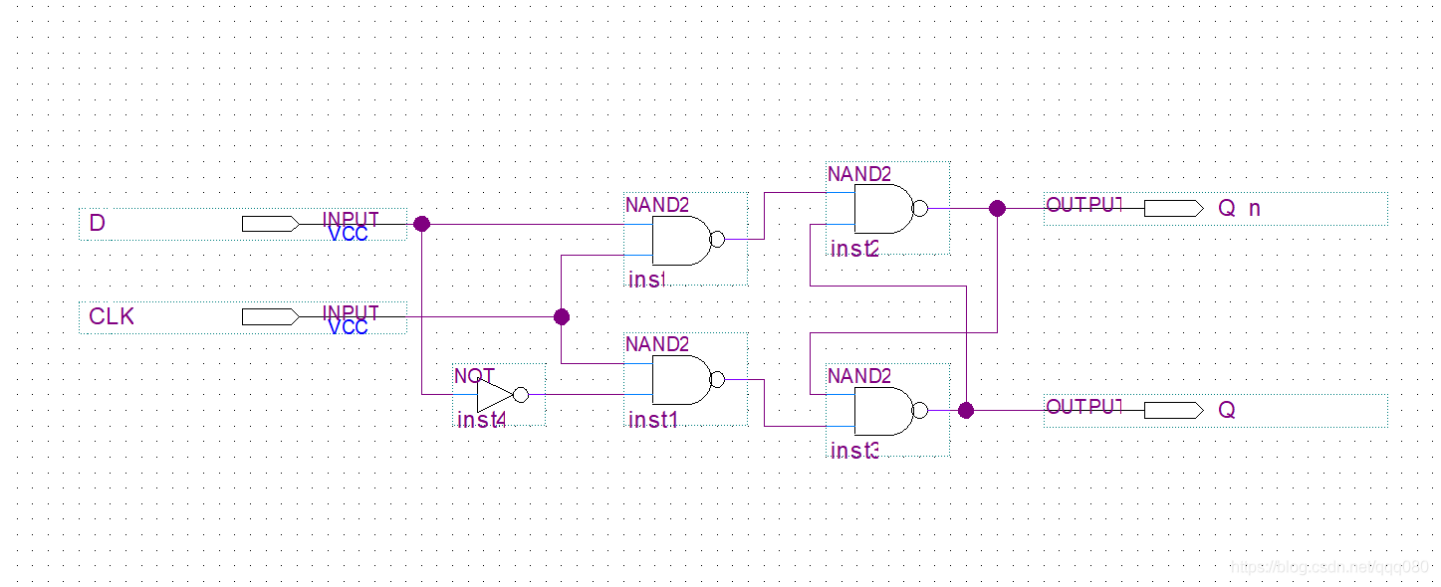
先点击File——》new
然后如下







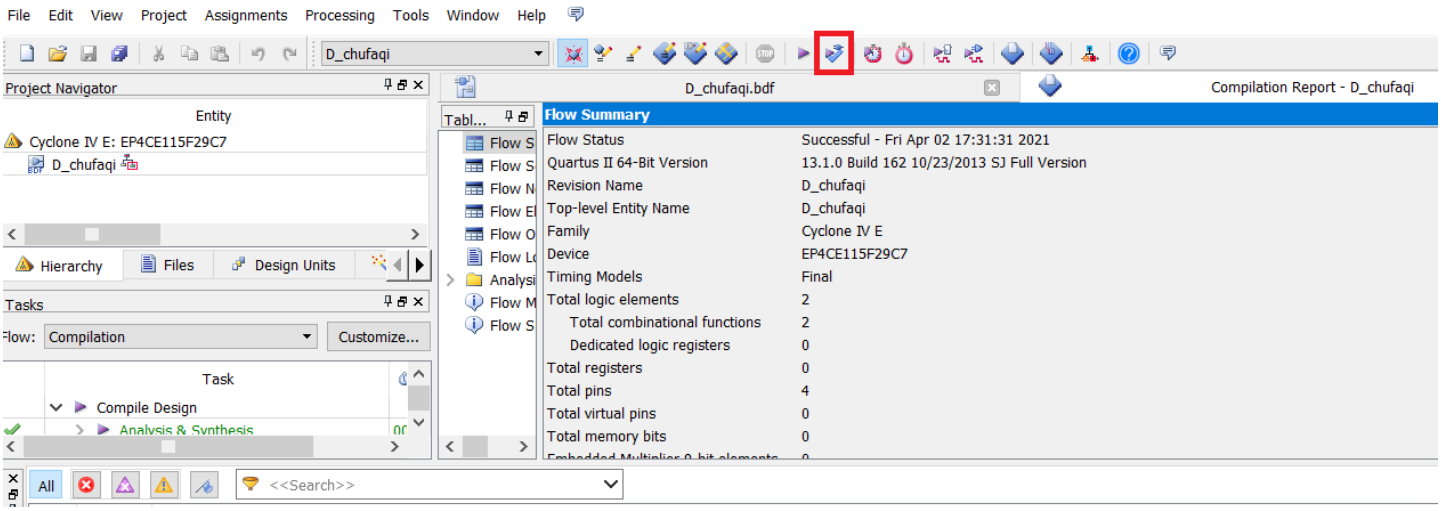
电路图如下



然后点击左上角的保存按钮保存。

3.编译原理图

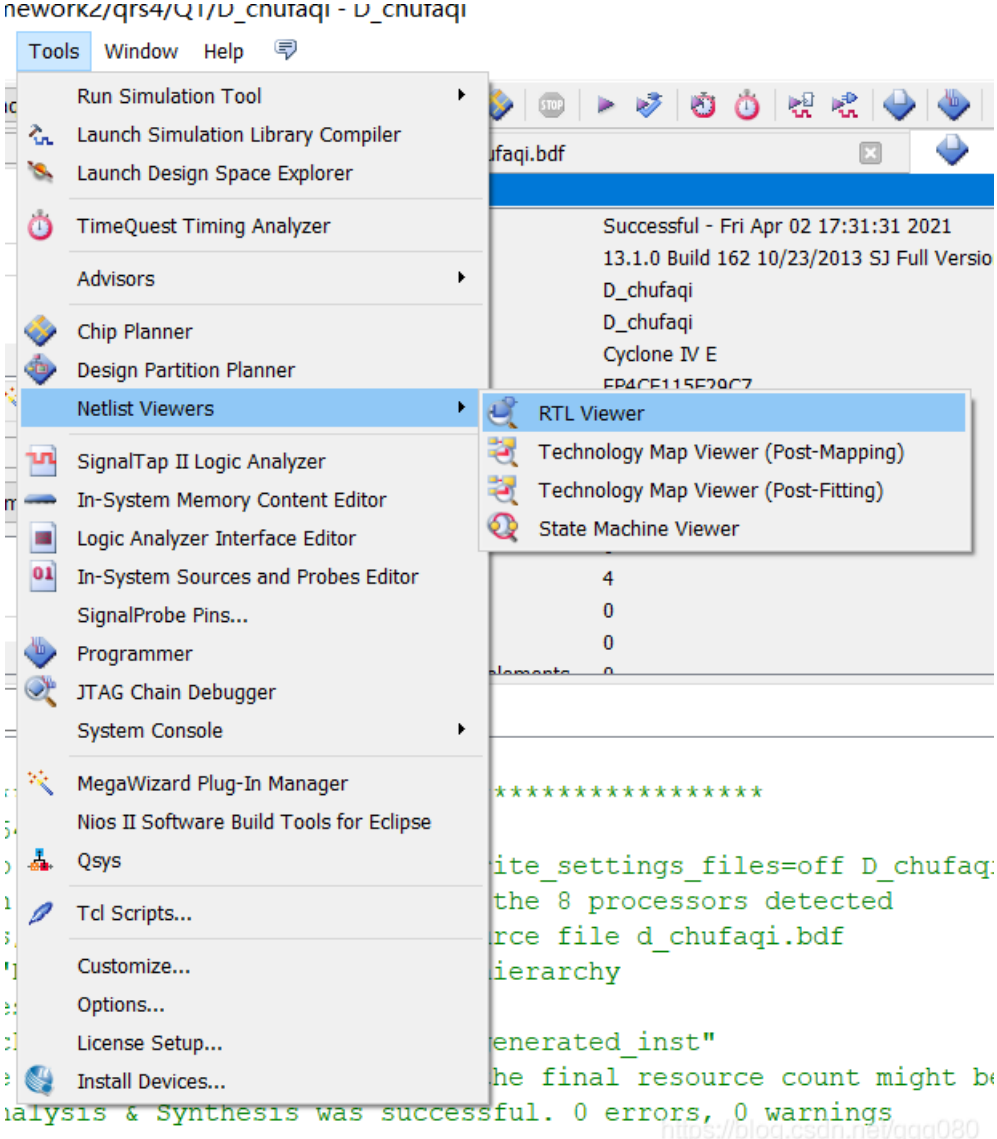
启动编译，无错误后

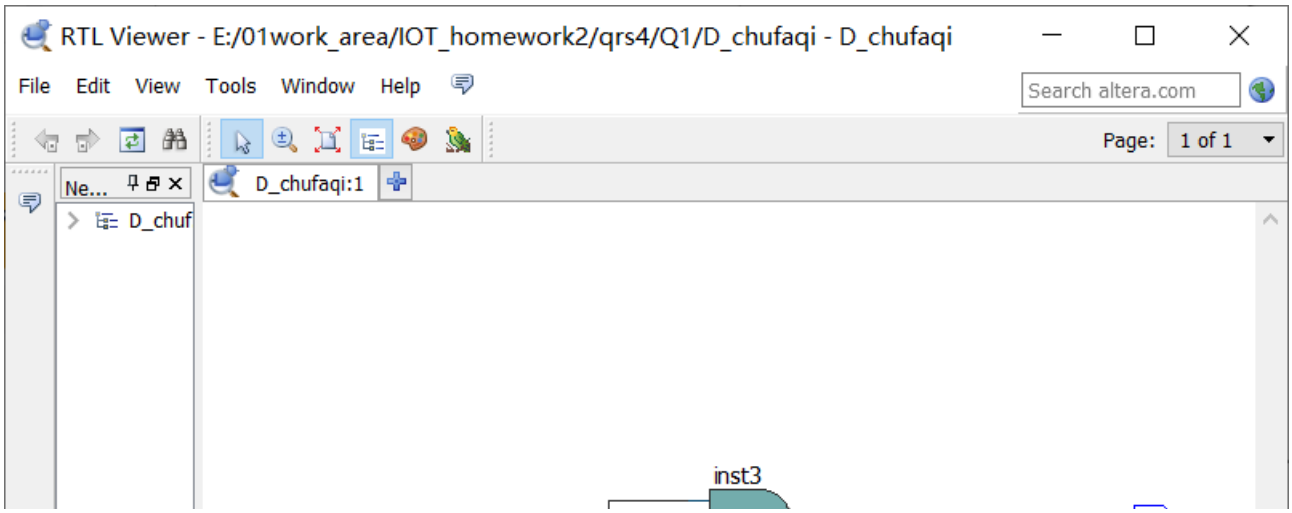


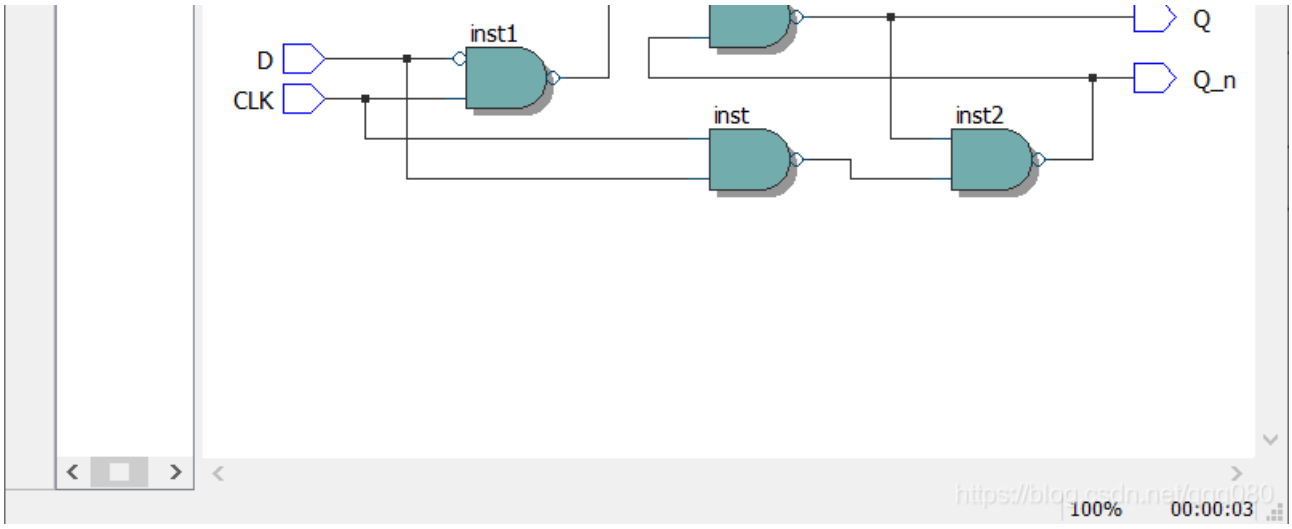
```
Type    ID     Message
        ******************************************************************
        Running Quartus II 64-Bit Analysis & Synthesis
        Command: quartus_map --read_settings_files=on --write_settings_files=off D_chufaqi -c D_chufaqi
20030   Parallel compilation is enabled and will use 8 of the 8 processors detected
12021   Found 1 design units, including 1 entities, in source file d_chufaqi.bdf
12127   Elaborating entity "D_chufaqi" for the top level hierarchy
286030  Timing-Driven Synthesis is running
16010   Generating hard_block partition "hard_block:auto_generated_inst"
21057   Implemented 6 device resources after synthesis - the final resource count might be different
        Quartus II 64-Bit Analysis & Synthesis was successful. 0 errors, 0 warnings
```

https://blog.csdn.net/qqq080

查看硬件电路图：点击Tools——》Netlist Viewers——》RTL Viewer

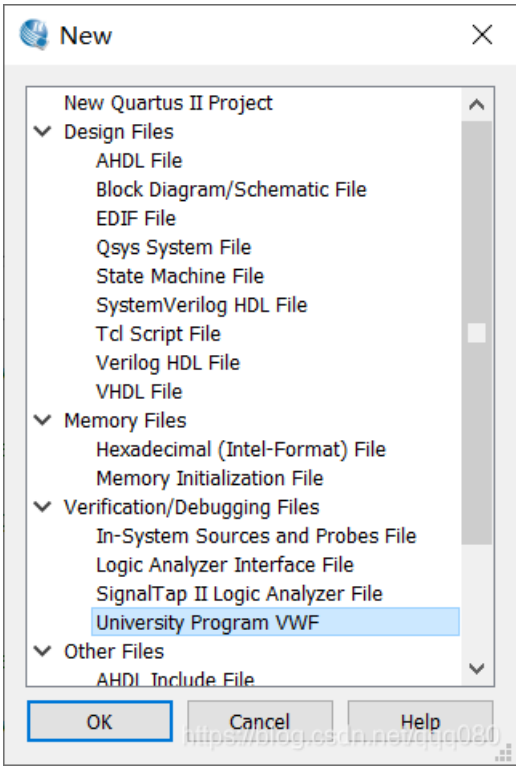




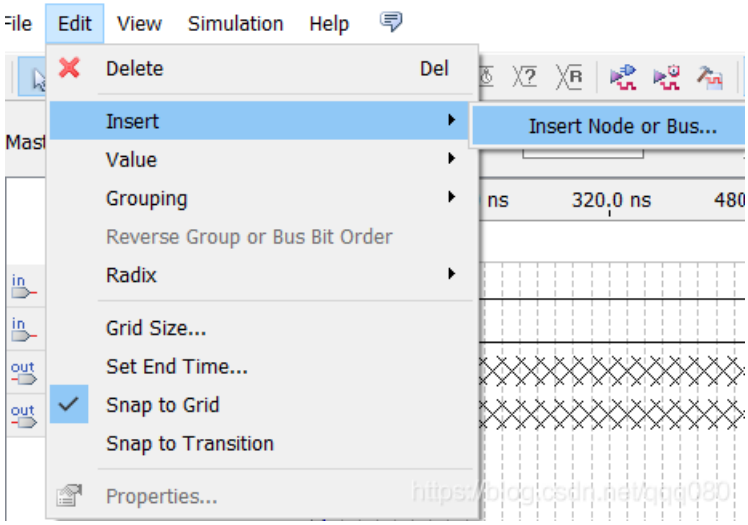


4.创建VWF文件

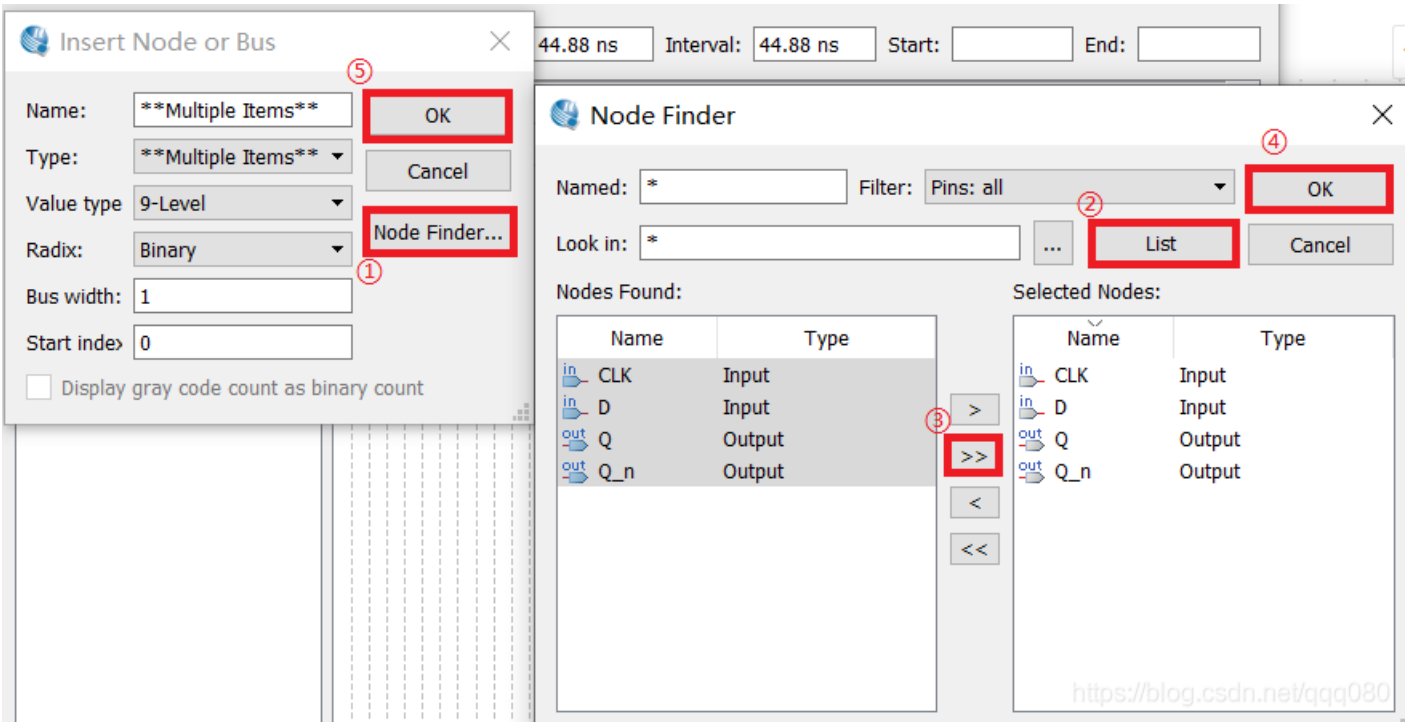
点击File——》new——》University Program VWF

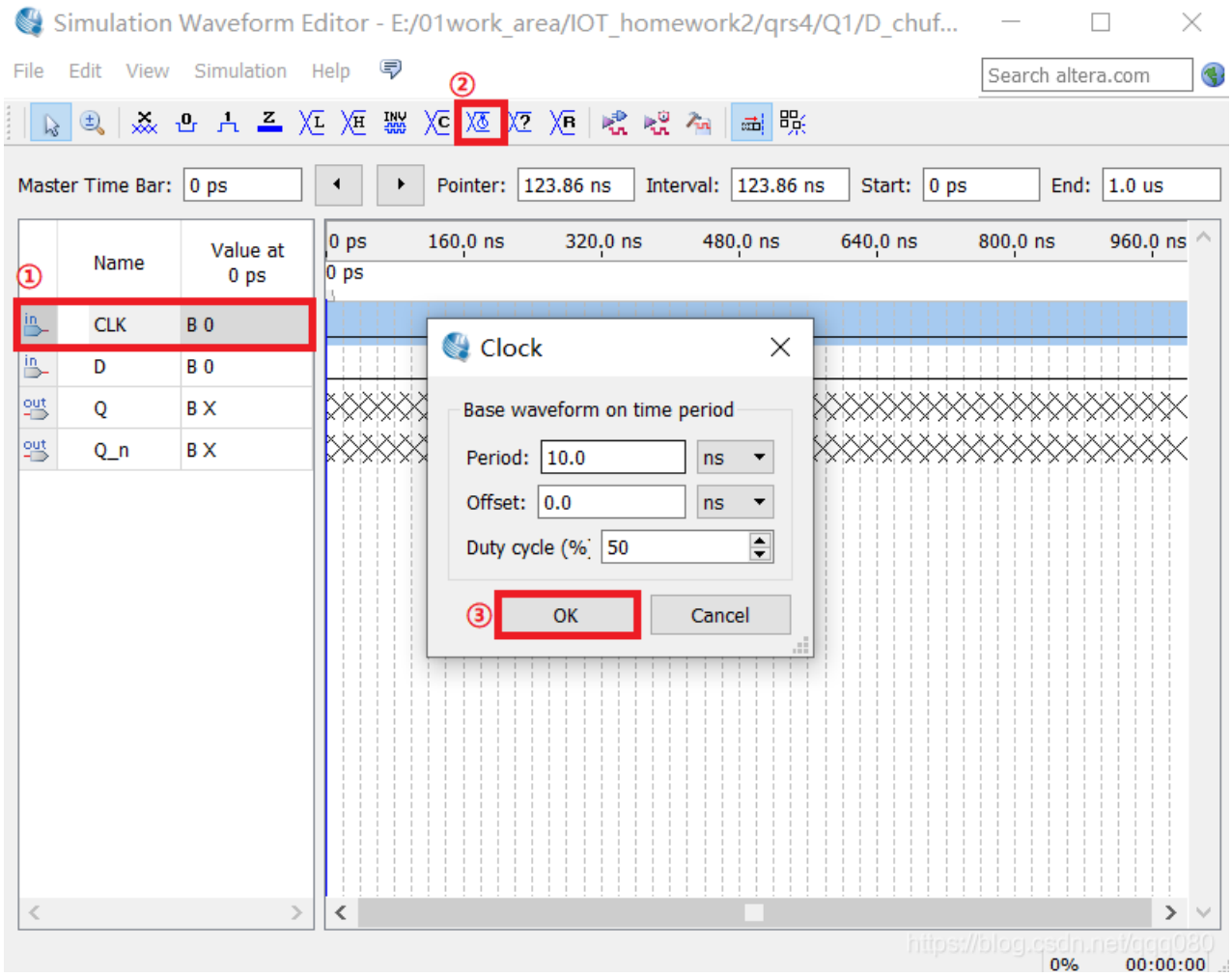


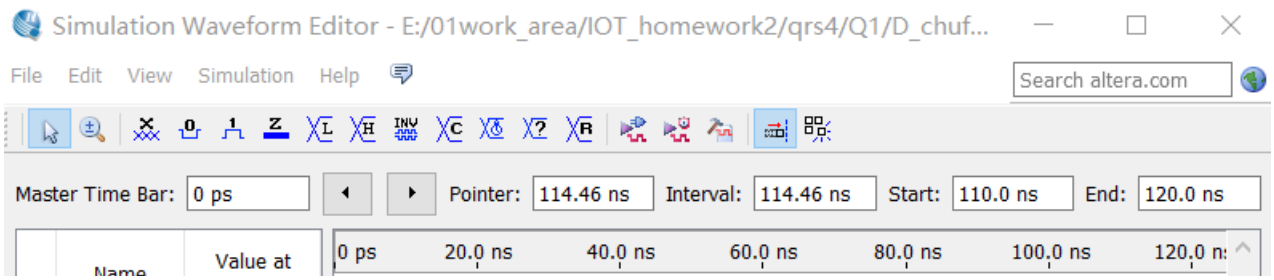
点击Edit——》Insert——》Insert Node or Bus…

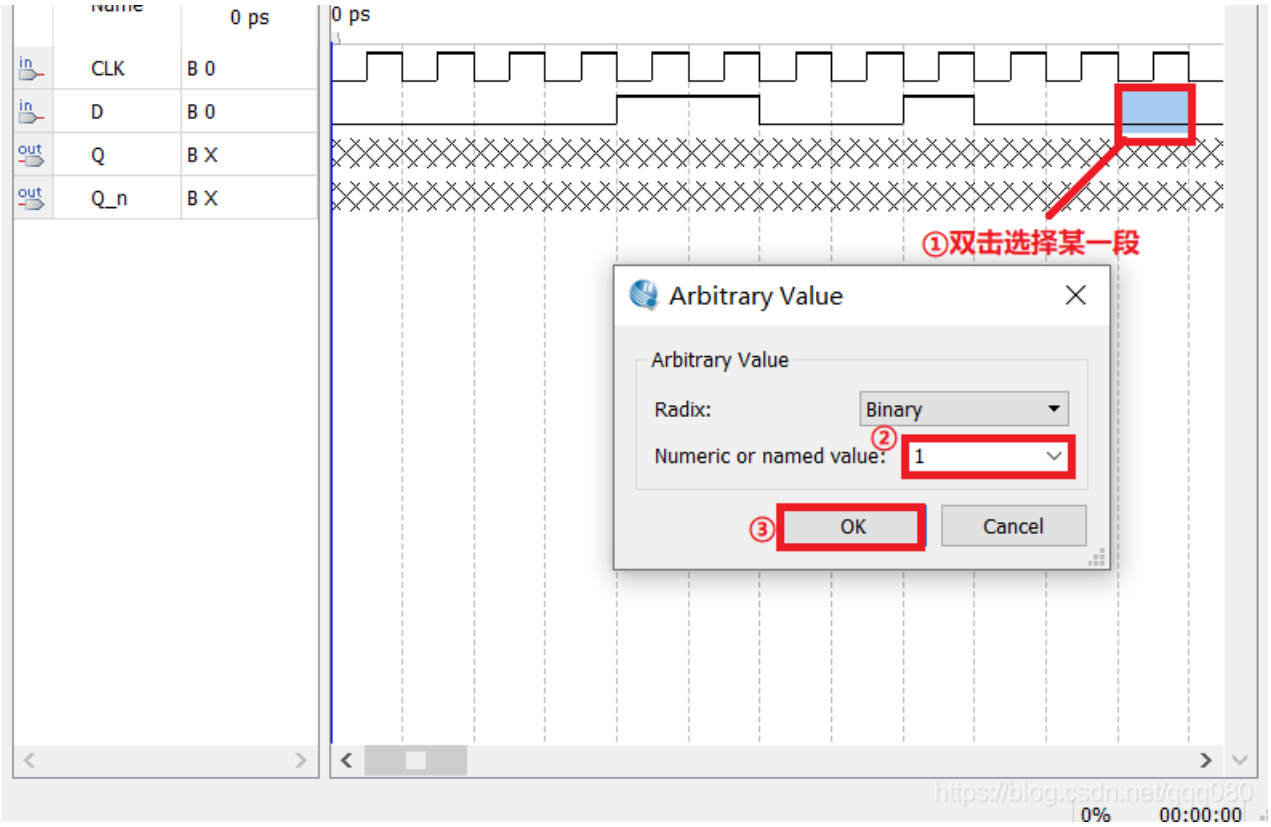


然后按照以下操作


Insert Node or Bus
Name: **Multiple Items**
Type: **Multiple Items**
Value type 9-Level
Radix: Binary
Bus width: 1
Start index: 0
Display gray code count as binary count
OK
Cancel
Node Finder...
Node Finder
Named: *
Filter: Pins: all
Look in: *
List
Nodes Found:
Name Type
CLK Input
D Input
Q Output
Q_n Output
Selected Nodes:
https://blog.csdn.net/qqq080


Simulation Waveform Editor - E:/01work_area/IOT_homework2/qrs4/Q1/D_chuf...
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 123.86 ns
Interval: 123.86 ns
Start: 0 ps
End: 1.0 us
Name
Value at 0 ps
CLK B 0
D B 0
Q B X
Q_n B X
0 ps 160.0 ns 320.0 ns 480.0 ns 640.0 ns 800.0 ns 960.0 ns
Clock
Base waveform on time period
Period: 10.0 ns
Offset: 0.0 ns
Duty cycle (%): 50
OK
Cancel
https://blog.csdn.net/qqq080
0% 00:00:00

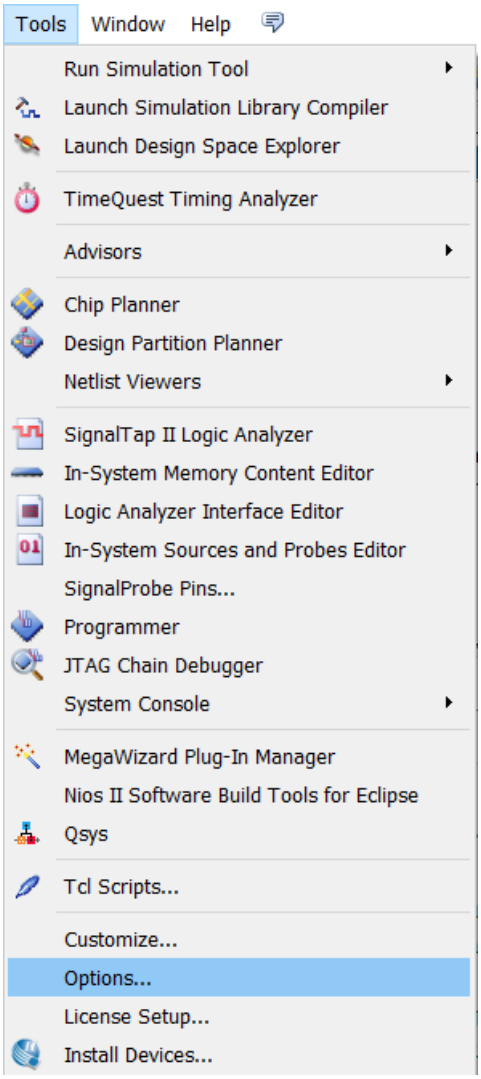

Simulation Waveform Editor - E:/01work_area/IOT_homework2/qrs4/Q1/D_chuf...
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 114.46 ns
Interval: 114.46 ns
Start: 110.0 ns
End: 120.0 ns
Value at
0 ps 20.0 ns 40.0 ns 60.0 ns 80.0 ns 100.0 ns 120.0 ns

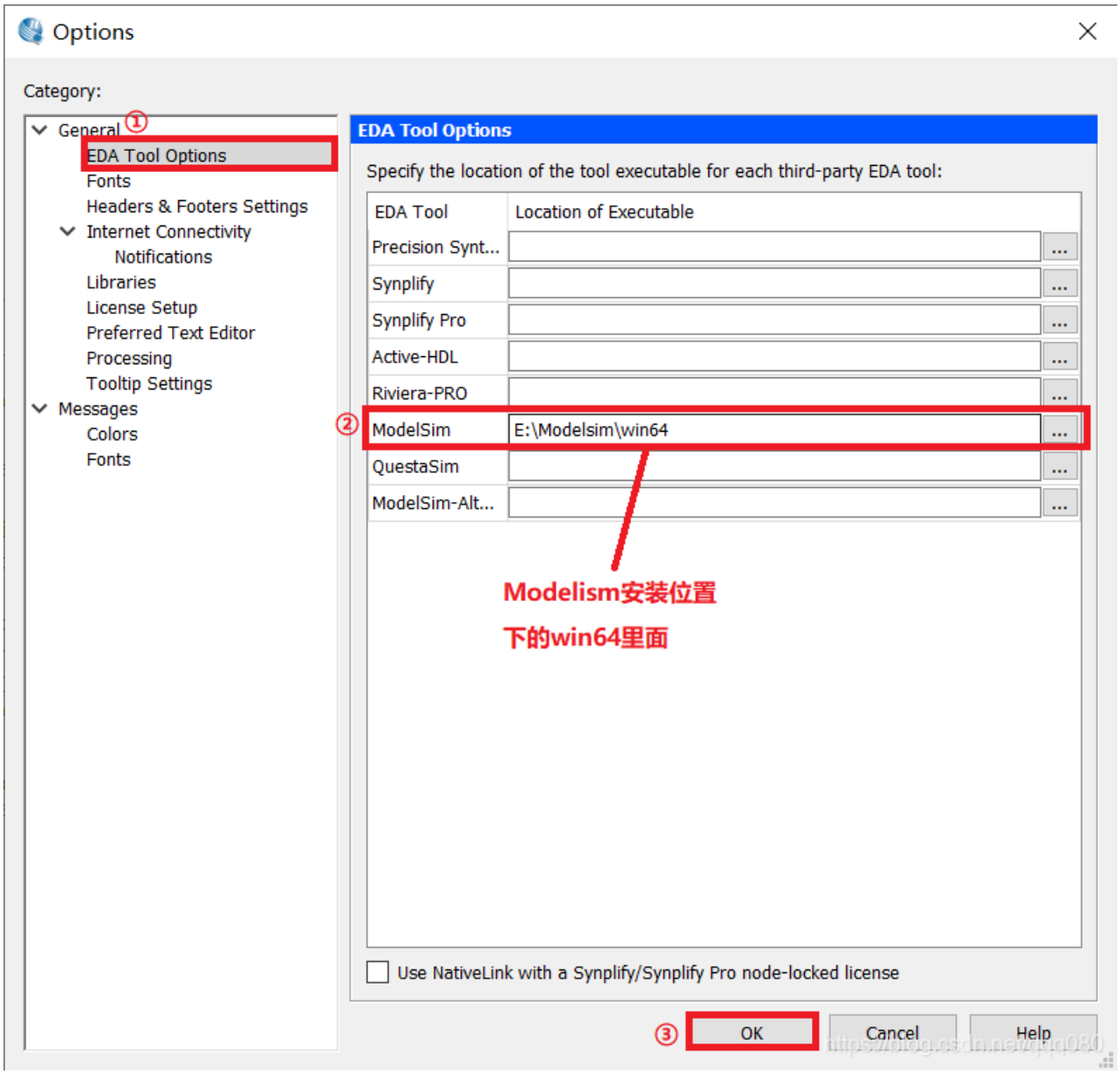


设置完成后保存文件，File——》Save

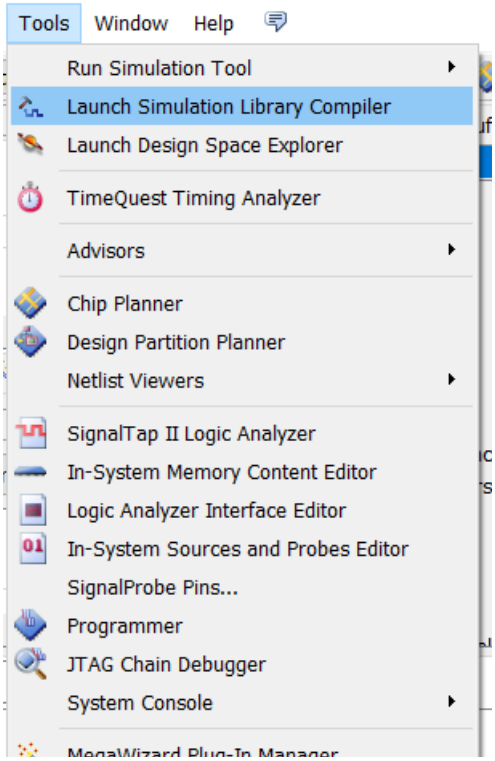
5.波形仿真

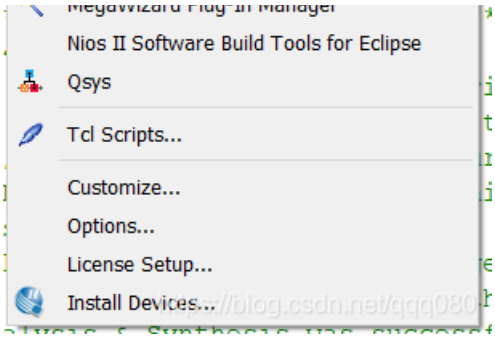
回到主界面，先将Modelism添加到编译器中

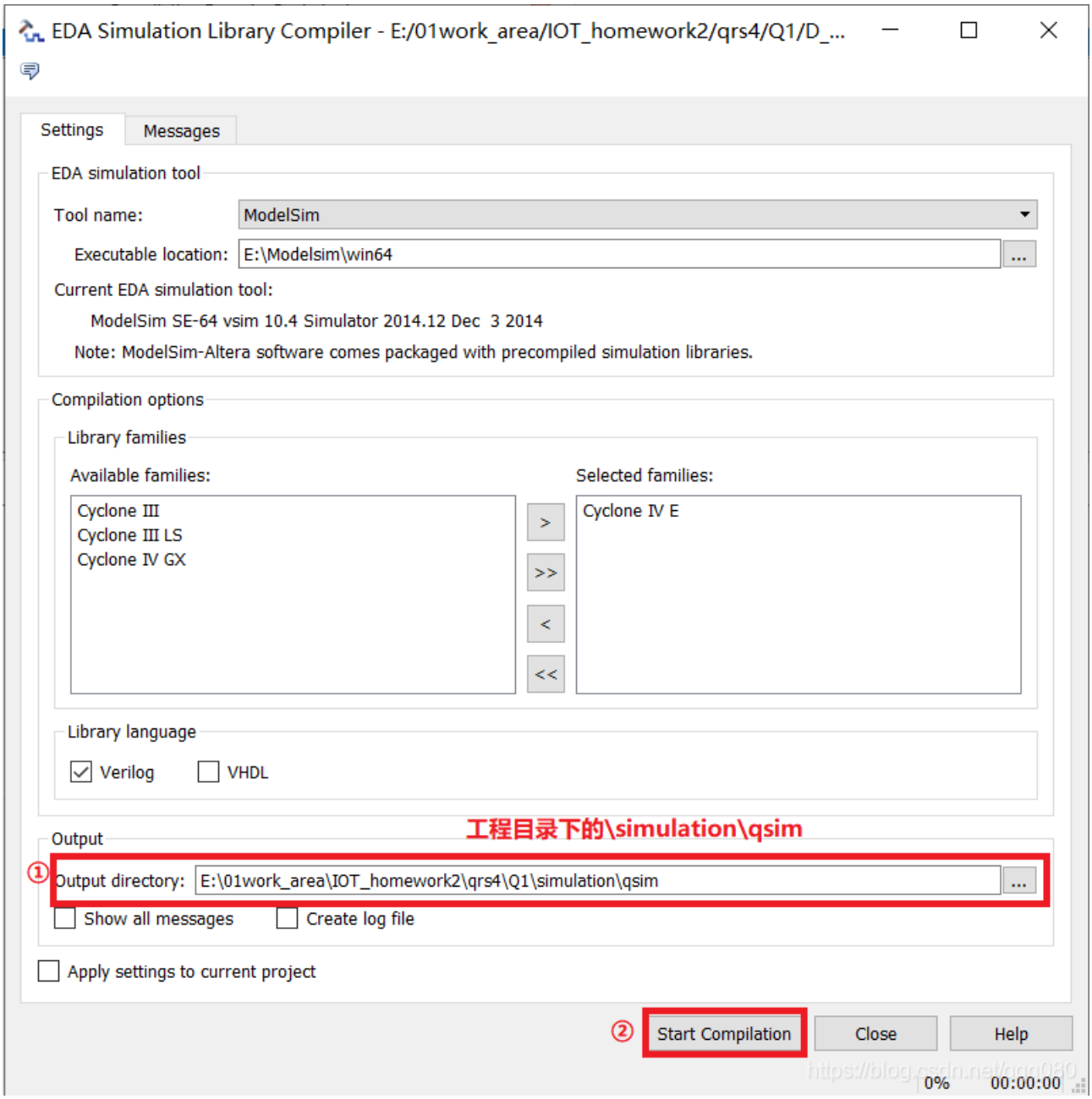


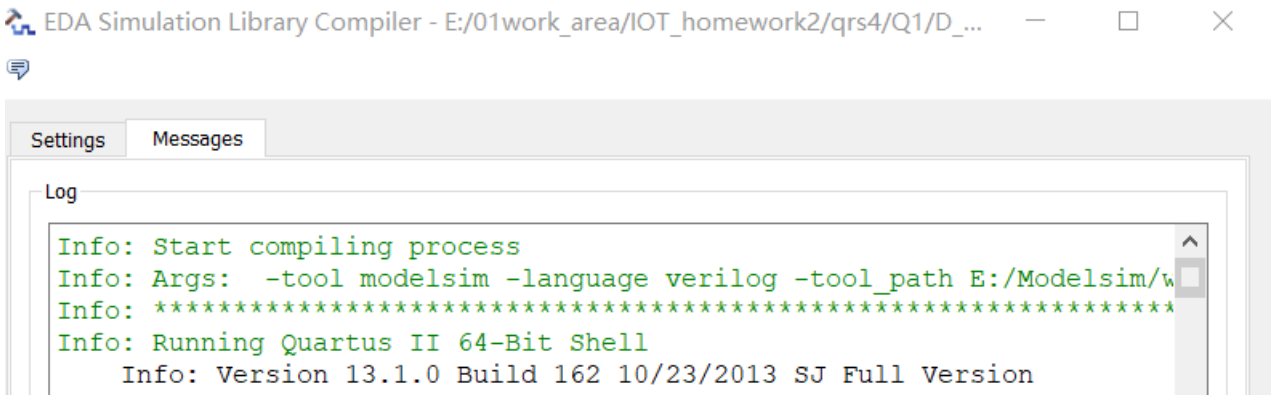


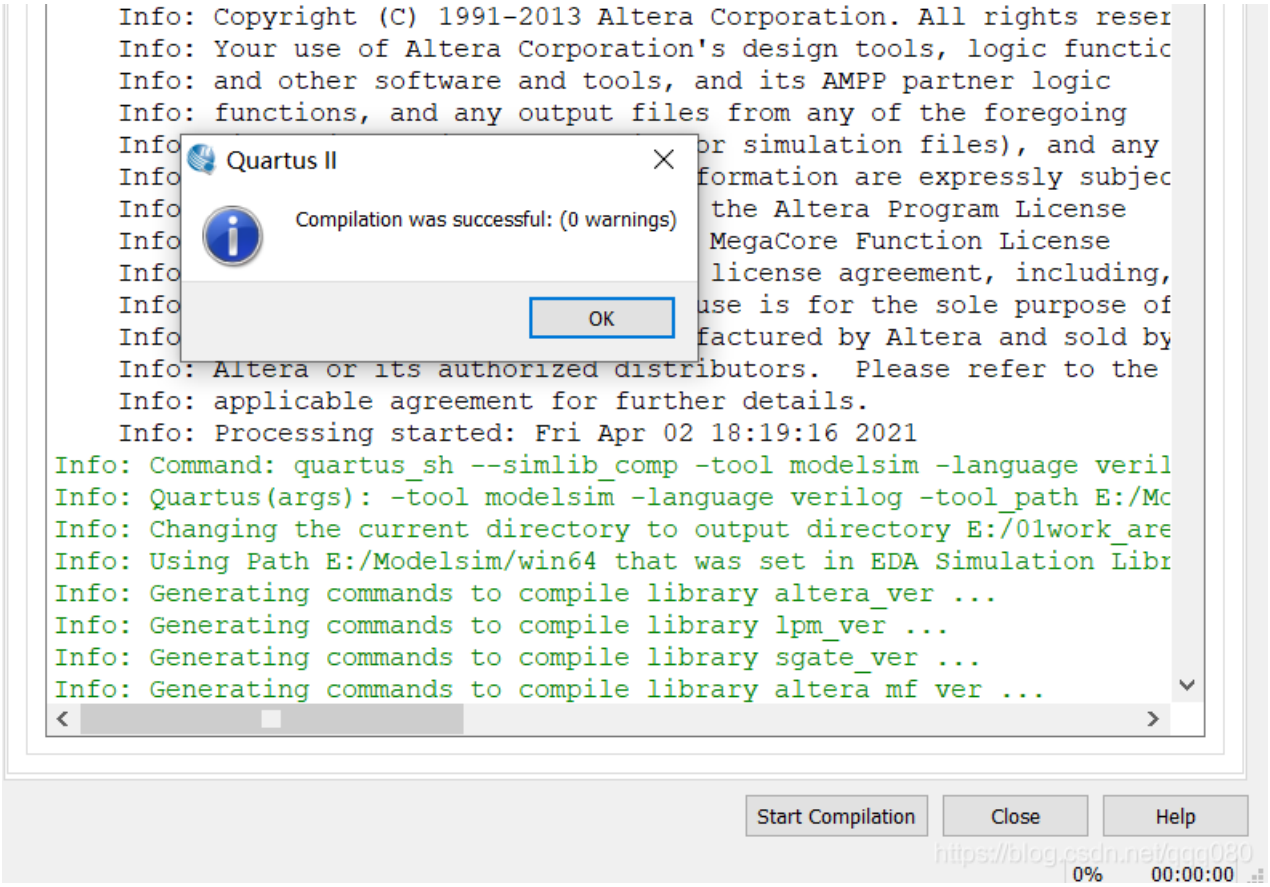
回到主界面，让编译器编译



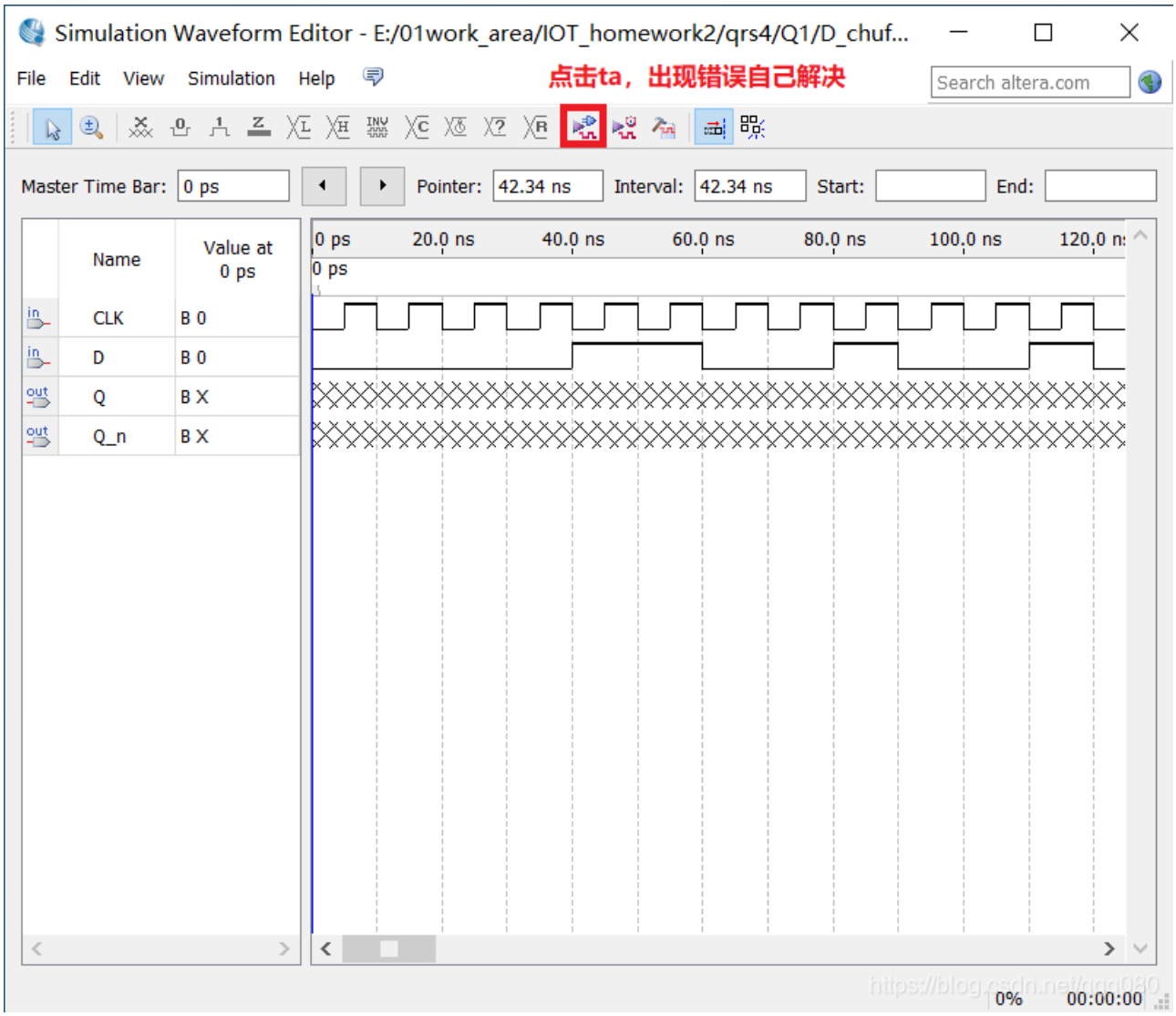

Nios II Software Build Tools for Eclipse
Qsys
Tcl Scripts...
Customize...
Options...
License Setup...
Install Devices...


EDA Simulation Library Compiler - E:/01work_area/IOT_homework2/qrs4/Q1/D_...
Settings
Messages
EDA simulation tool
Tool name:
ModelSim
Executable location:
E:\Modelsim\win64
Current EDA simulation tool:
ModelSim SE-64 vsim 10.4 Simulator 2014.12 Dec 3 2014
Note: ModelSim-Altera software comes packaged with precompiled simulation libraries.
Compilation options
Library families
Available families:
Cyclone III
Cyclone III LS
Cyclone IV GX
Selected families:
Cyclone IV E
Library language
Verilog
VHDL
工程目录下的\simulation\qsim
Output
①
Output directory:
E:\01work_area\IOT_homework2\qrs4\Q1\simulation\qsim
Show all messages
Create log file
Apply settings to current project
②
Start Compilation
Close
Help
0%
00:00:00

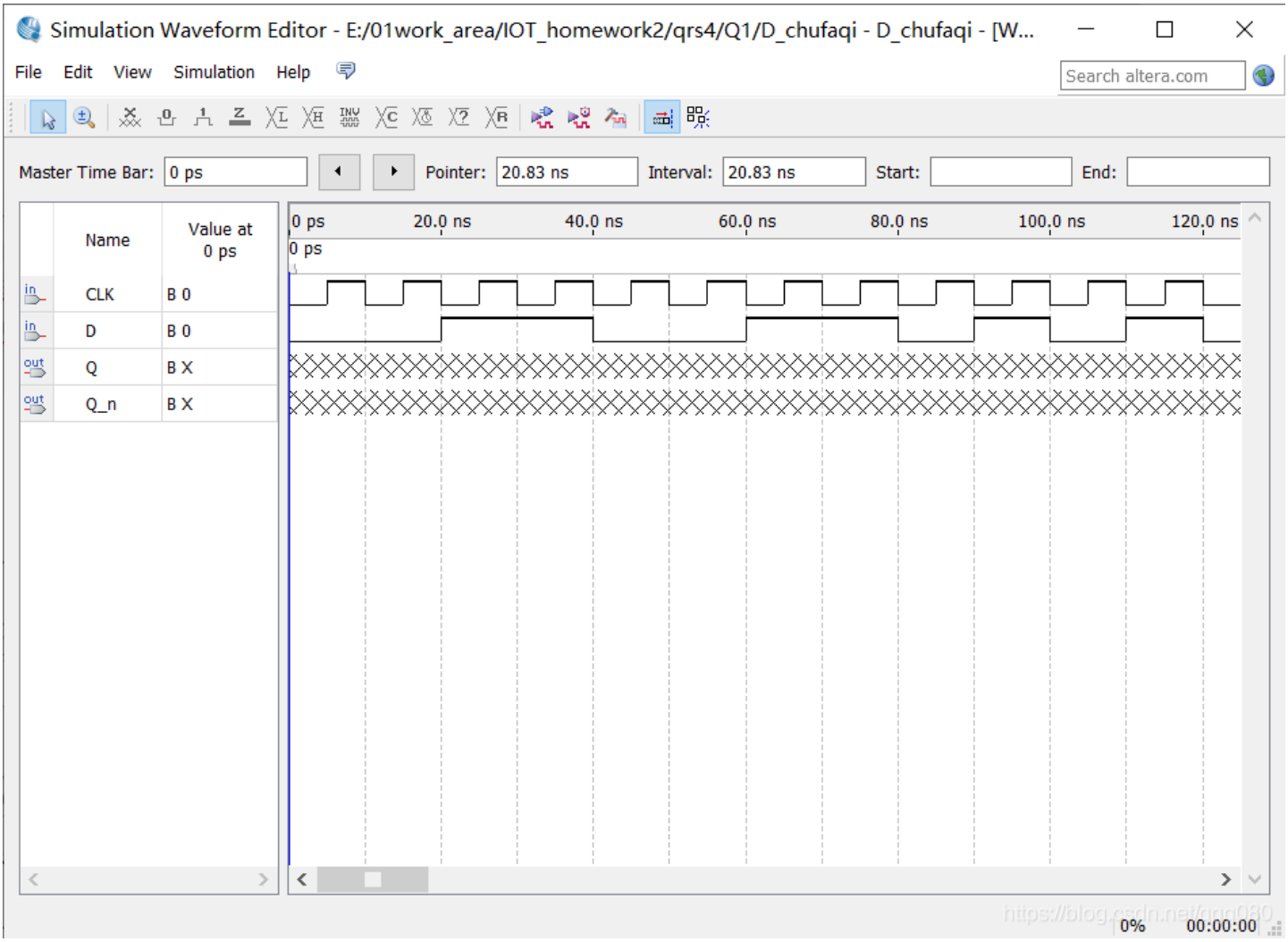

EDA Simulation Library Compiler - E:/01work_area/IOT_homework2/qrs4/Q1/D_...
Settings
Messages
Log
Info: Start compiling process
Info: Args: -tool modelsim -language verilog -tool_path E:/Modelsim/w
Info: **********
Info: Running Quartus II 64-Bit Shell
Info: Version 13.1.0 Build 162 10/23/2013 SJ Full Version


Info: Copyright (C) 1991-2013 Altera Corporation. All rights reser
Info: Your use of Altera Corporation's design tools, logic functic
Info: and other software and tools, and its AMPP partner logic
Info: functions, and any output files from any of the foregoing
Info: Altera or its authorized distributors. Please refer to the
Info: applicable agreement for further details.
Info: Processing started: Fri Apr 02 18:19:16 2021
Info: Command: quartus_sh --simlib_comp -tool modelsim -language veril
Info: Quartus(args): -tool modelsim -language verilog -tool_path E:/Mc
Info: Changing the current directory to output directory E:/01work_are
Info: Using Path E:/Modelsim/win64 that was set in EDA Simulation Libr
Info: Generating commands to compile library altera_ver ...
Info: Generating commands to compile library lpm_ver ...
Info: Generating commands to compile library sgate_ver ...
Info: Generating commands to compile library altera mf ver ...
Quartus II
Compilation was successful: (0 warnings)
OK
Start Compilation
Close
Help
0%
00:00:00

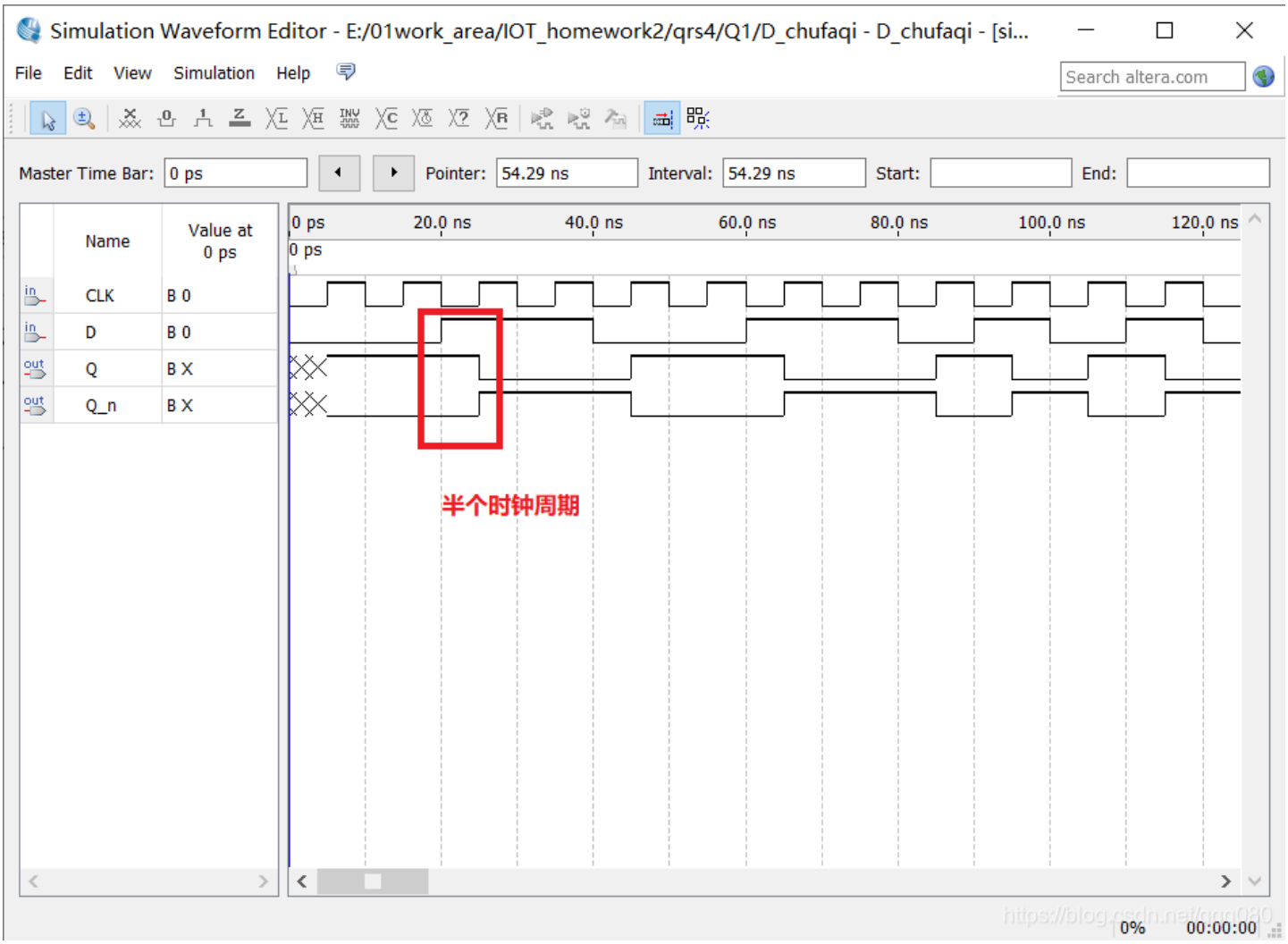
无错误后


Simulation Waveform Editor - E:/01work_area/IOT_homework2/qrs4/Q1/D_chuf...
File Edit View Simulation Help
点击ta，出现错误自己解决
Search altera.com
Master Time Bar: 0 ps
Pointer: 42.34 ns
Interval: 42.34 ns
Start:
End:
Name
Value at 0 ps
CLK
D
Q
Q_n
B 0
B 0
B X
B X
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 n
0%
00:00:00

为了同后面对比，这里吧D输入调成一样的



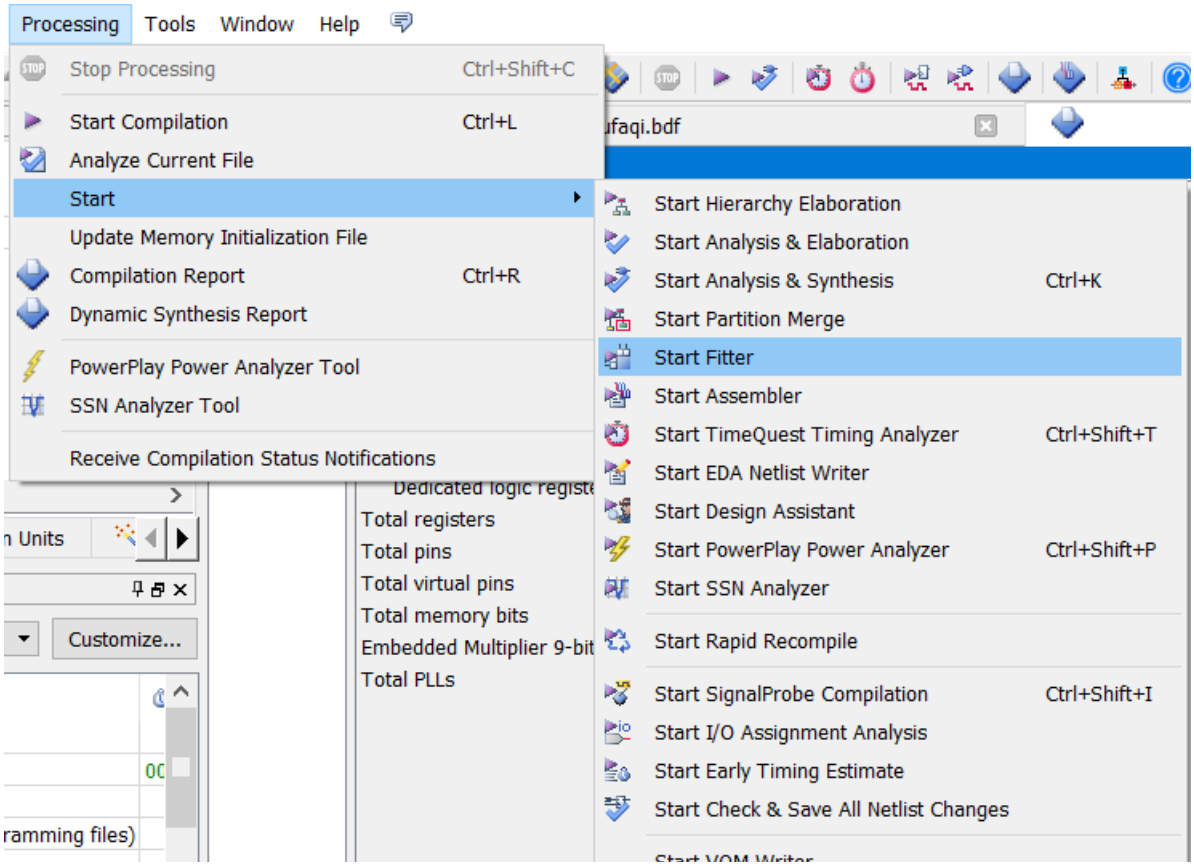
功能仿真

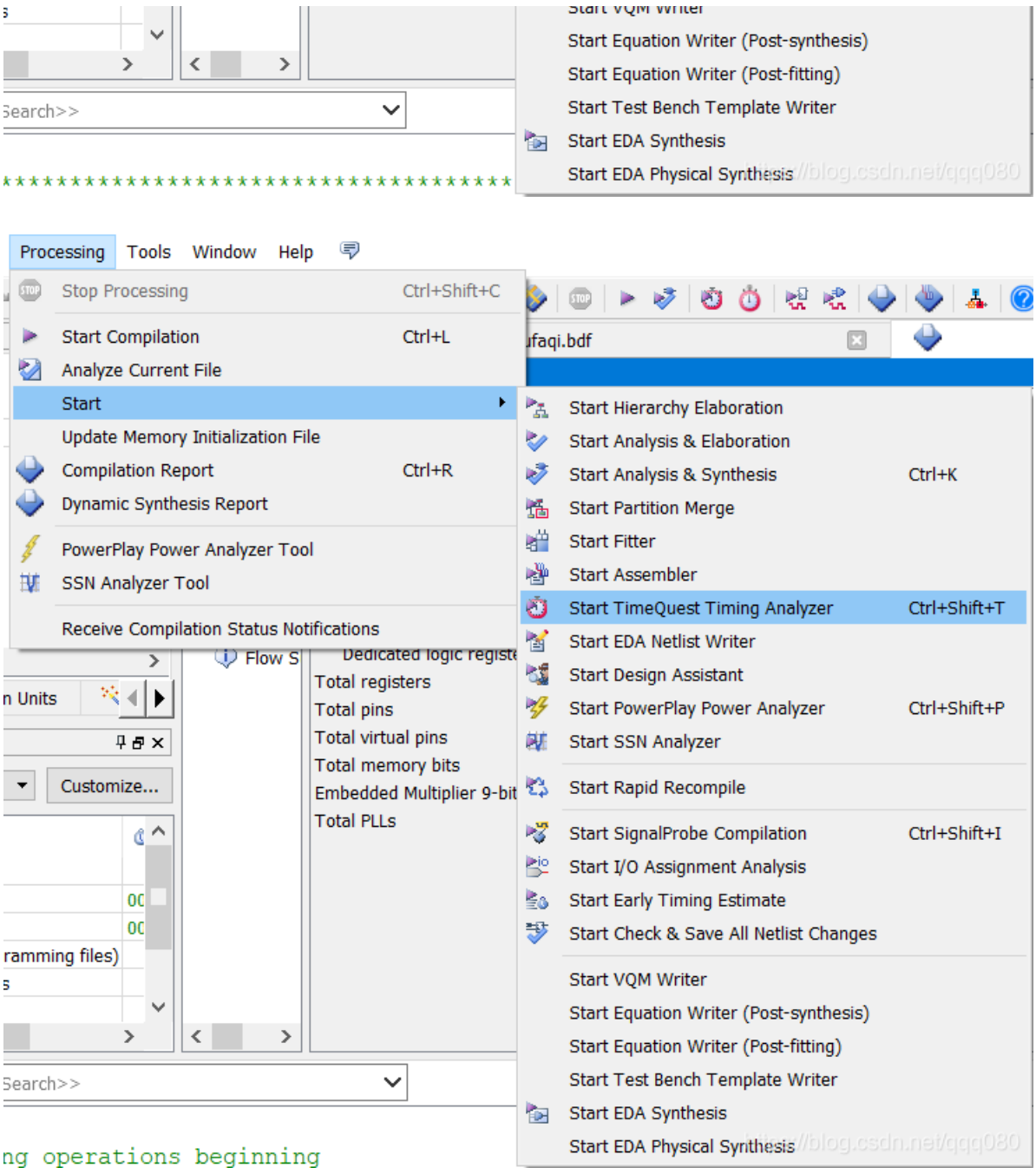


时序仿真

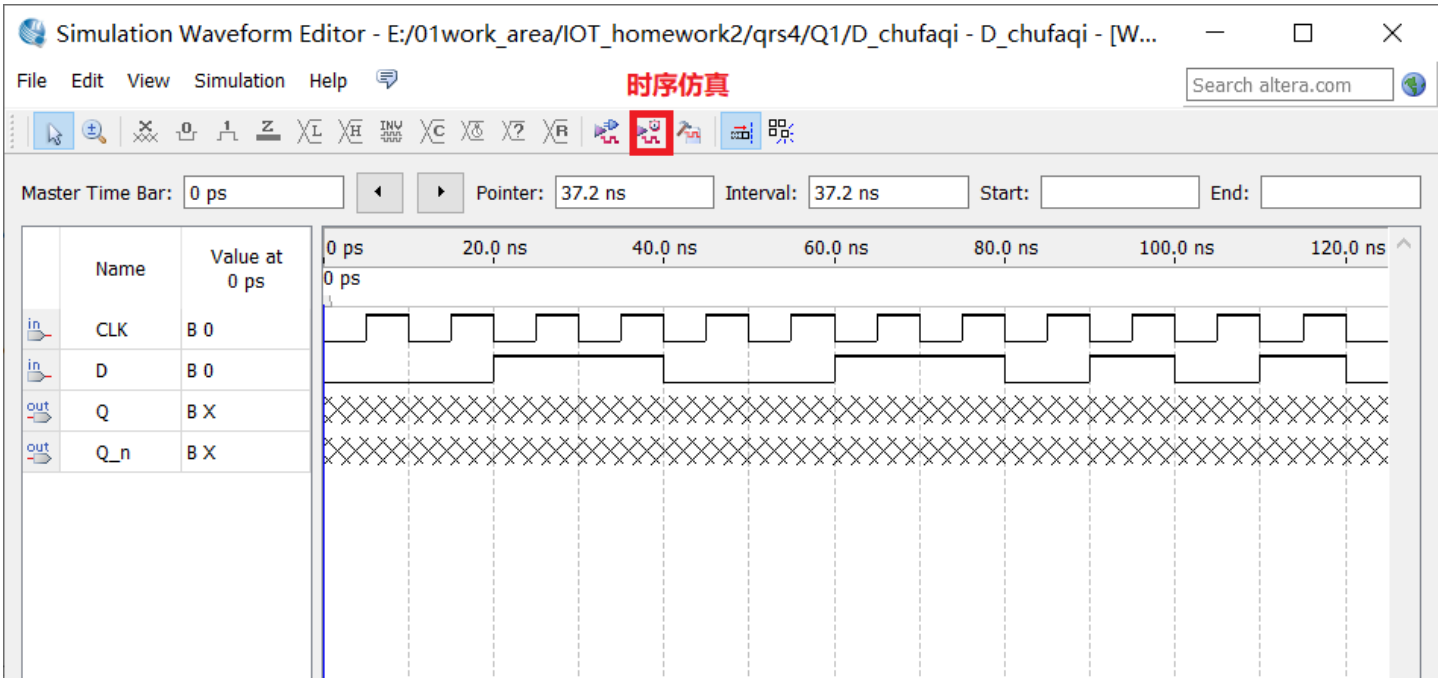
需要一下操作

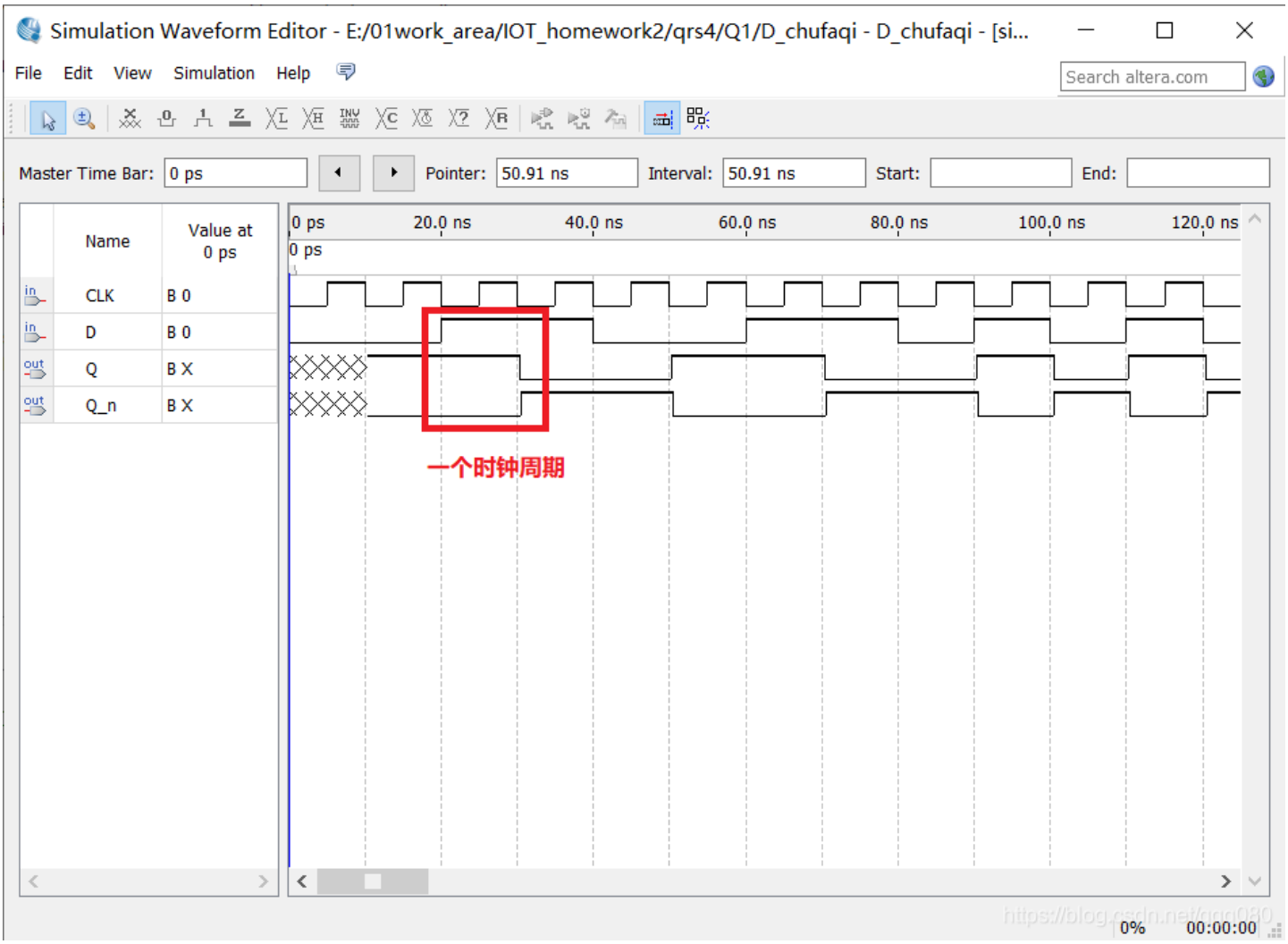
到主界面点击




Start Equation Writer (Post-synthesis)
Start Equation Writer (Post-fitting)
Start Test Bench Template Writer
Start EDA Synthesis
Start EDA Physical Synthesis
Processing
Tools
Window
Help
Stop Processing Ctrl+Shift+C
Start Compilation Ctrl+L
Analyze Current File
Start
Update Memory Initialization File
Compilation Report Ctrl+R
Dynamic Synthesis Report
PowerPlay Power Analyzer Tool
SSN Analyzer Tool
Receive Compilation Status Notifications
Start Hierarchy Elaboration
Start Analysis & Elaboration
Start Analysis & Synthesis Ctrl+K
Start Partition Merge
Start Fitter
Start Assembler
Start TimeQuest Timing Analyzer Ctrl+Shift+T
Start EDA Netlist Writer
Start Design Assistant
Start PowerPlay Power Analyzer Ctrl+Shift+P
Start SSN Analyzer
Start Rapid Recompile
Start SignalProbe Compilation Ctrl+Shift+I
Start I/O Assignment Analysis
Start Early Timing Estimate
Start Check & Save All Netlist Changes
Start VQM Writer
Start Equation Writer (Post-synthesis)
Start Equation Writer (Post-fitting)
Start Test Bench Template Writer
Start EDA Synthesis
Start EDA Physical Synthesis
Total registers
Total pins
Total virtual pins
Total memory bits
Embedded Multiplier 9-bit
Total PLLs
Customize...
ng operations beginning

然后到VMF中，


Simulation Waveform Editor - E:/01work_area/IOT_homework2/qrs4/Q1/D_chufaqi - D_chufaqi - [W...
File Edit View Simulation Help
时序仿真
Search altera.com
Master Time Bar: 0 ps
Pointer: 37.2 ns
Interval: 37.2 ns
Start:
End:
Name
Value at 0 ps
CLK B 0
D B 0
Q B X
Q_n B X
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns



二、调用D触发器电路

1.新建工程

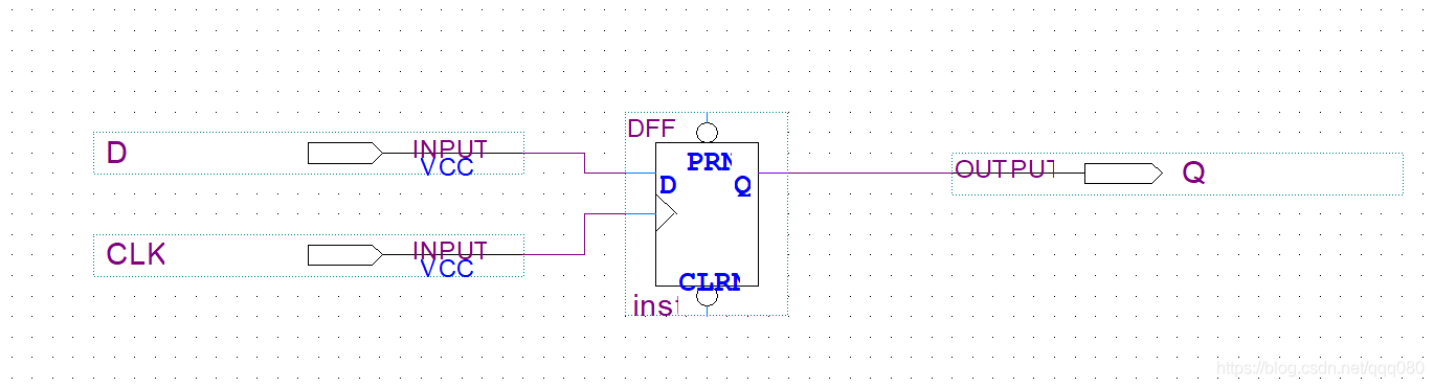
新建工程和上面的一样。

2.创建原理图

步骤一样，在选择器件时，直接选择D触发器。

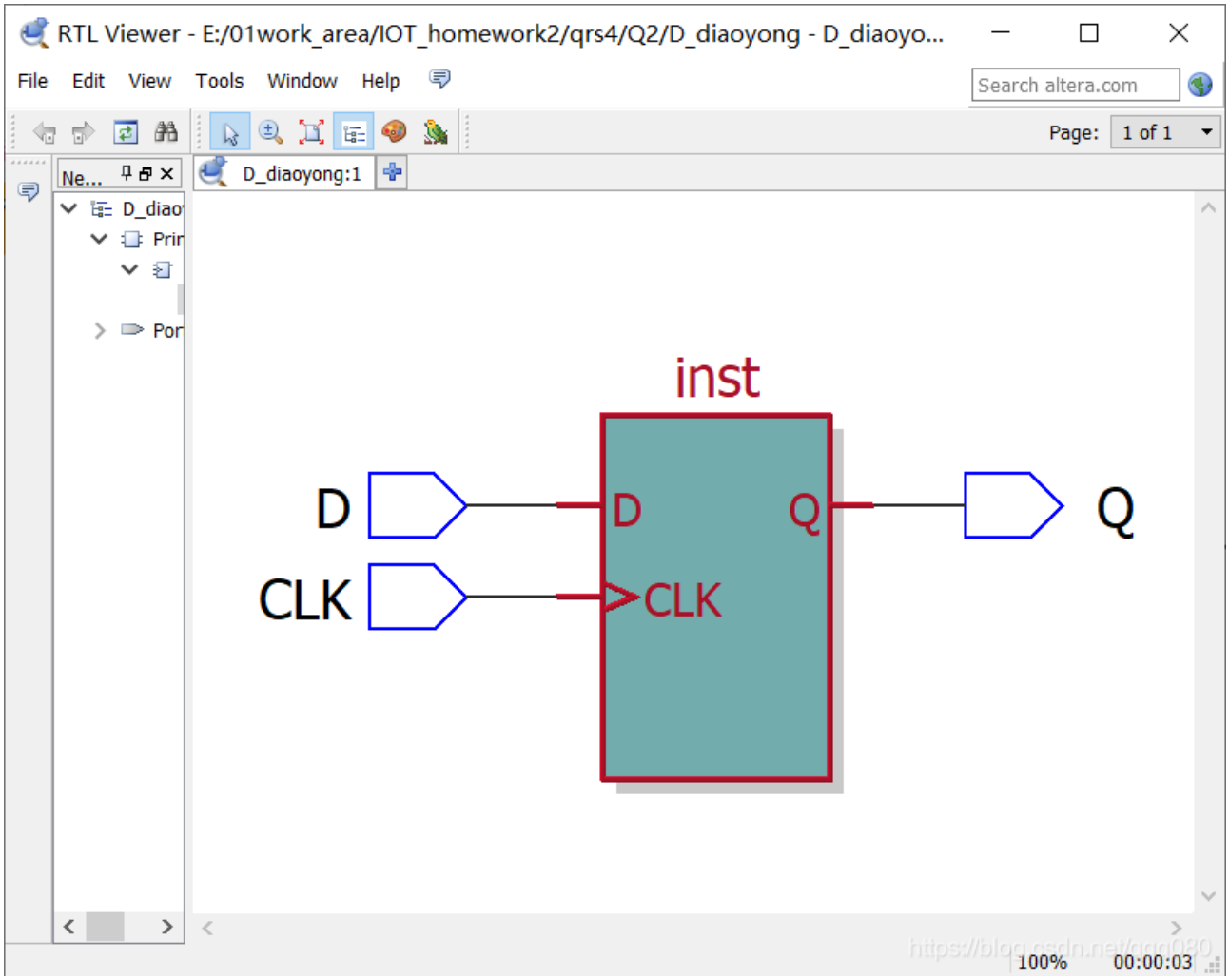
搜索`dff`，调用D触发器。

原理图如下



3.编译原理图

步骤一样，编译后查看一下原理图。



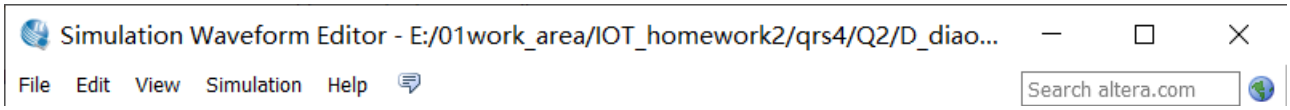
4.创建VWF文件

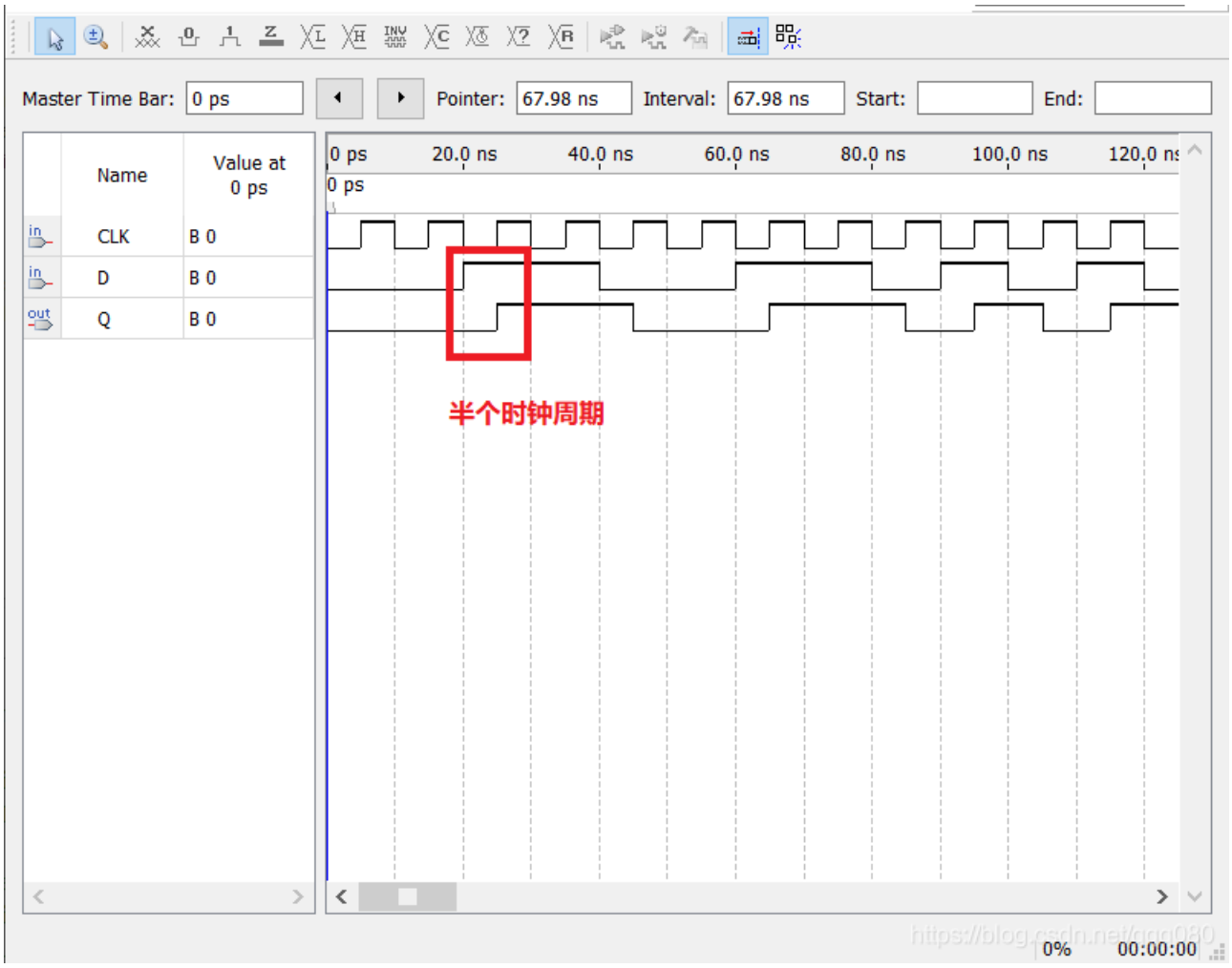
更上面步骤一样。

5.波形仿真

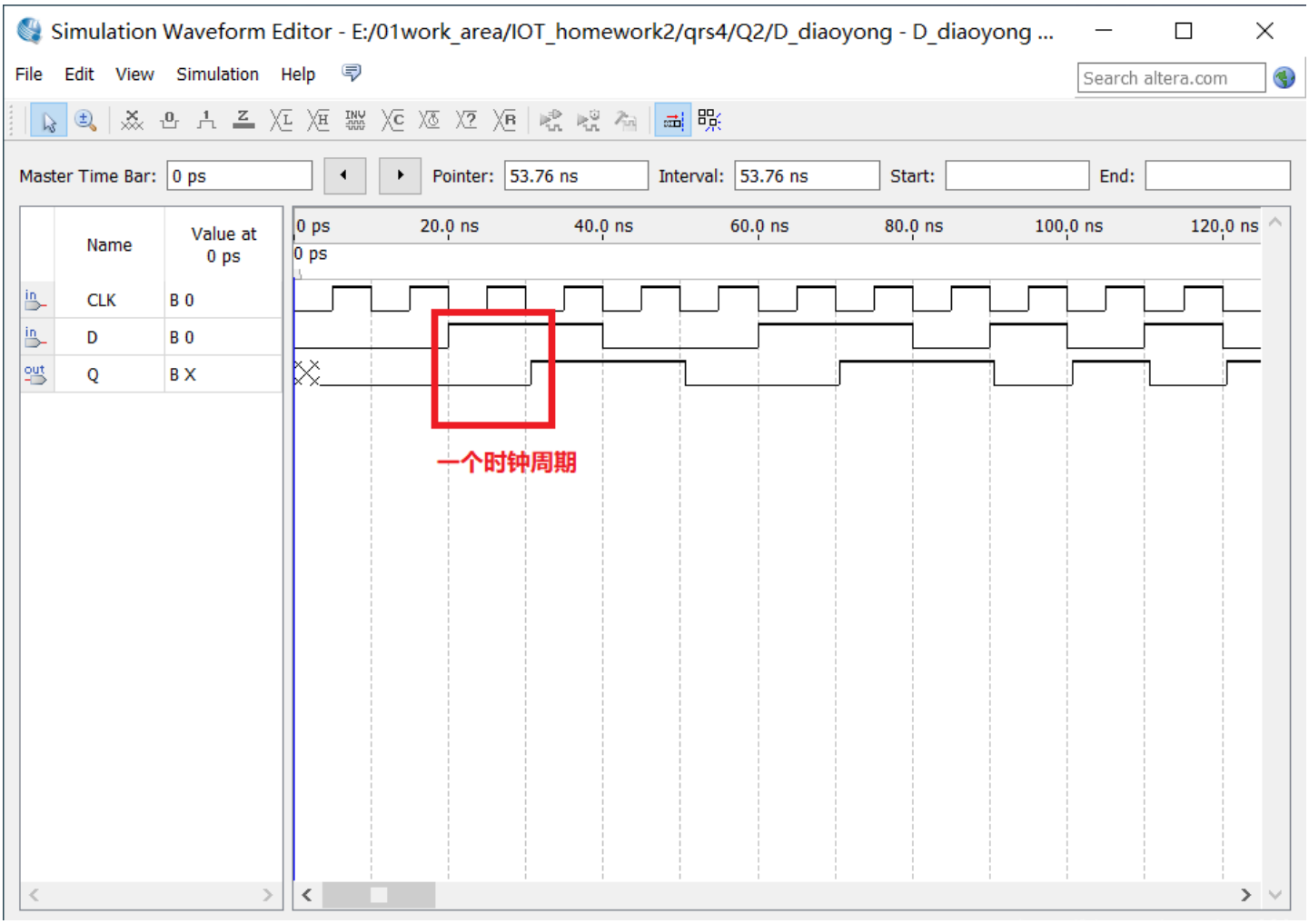
依然和上面一样。

功能仿真




Master Time Bar: 0 ps
Pointer: 67.98 ns
Interval: 67.98 ns
Start:
End:
Name
Value at 0 ps
CLK
B 0
D
B 0
Q
B 0
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
半个时钟周期
0%
00:00:00

时序仿真


Simulation Waveform Editor - E:/01work_area/IOT_homework2/qrs4/Q2/D_diaoyong - D_diaoyong ...
File
Edit
View
Simulation
Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 53.76 ns
Interval: 53.76 ns
Start:
End:
Name
Value at 0 ps
CLK
B 0
D
B 0
Q
B X
0 ps
20.0 ns
40.0 ns
60.0 ns
80.0 ns
100.0 ns
120.0 ns
一个时钟周期

https://blog.csdn.net/qq080

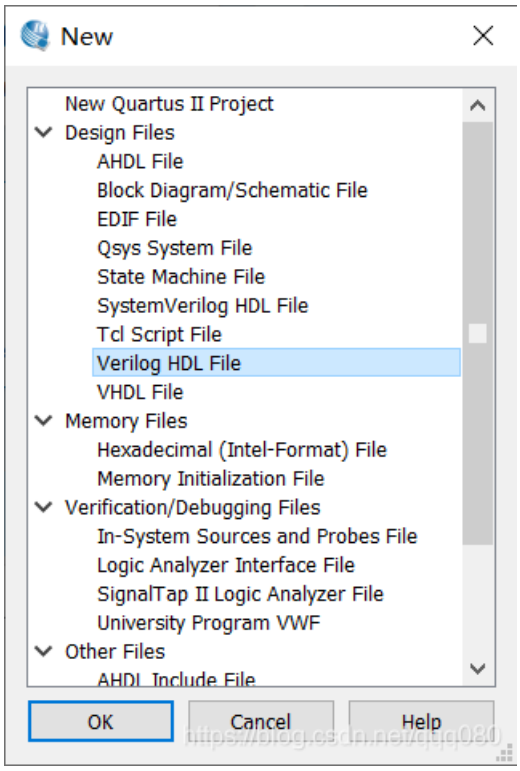
0% 00:00:00

三、用Verilog语言写D触发器

1.新建工程

依然和前面的一样

2.写Verilog文件



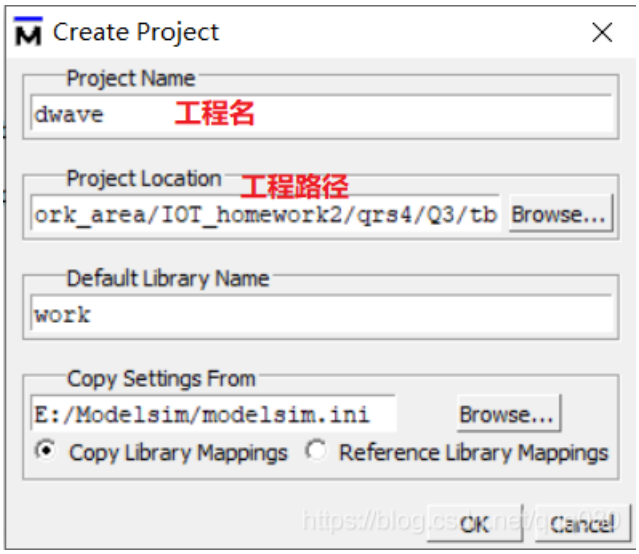
写入以下代码

```
//dwave是工程文件名，需要根据工程名来改变
module dwave(d,clk,q);
    input d;
    input clk;
    output q;

    reg q;

    always @ (posedge clk)//我们用正的时钟沿做它的敏感信号
    begin
        q <= d;//上升沿有效的时候，把d捕获到q
    end
endmodule
```

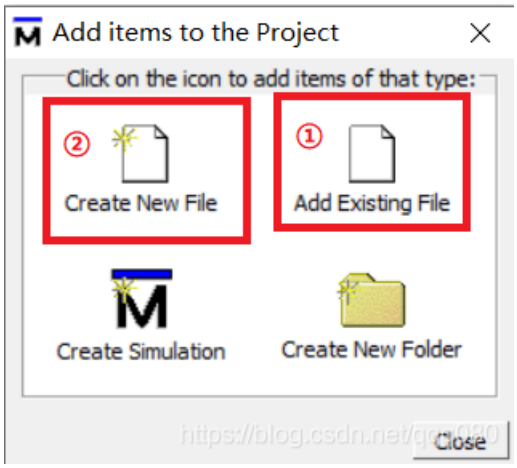
然后编译并保存

3.Modelism手动仿真

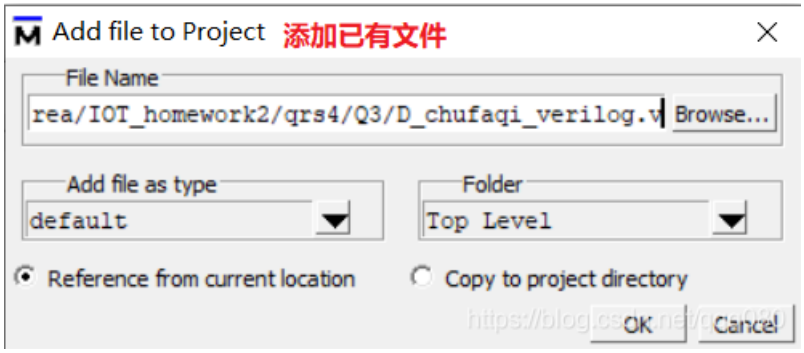
- 在刚刚创建的Quartus工程下创建tb文件夹
- 打开Modelism软件
- 点击File——》Change Directory——》选择tb文件夹
- File——》New——》Project



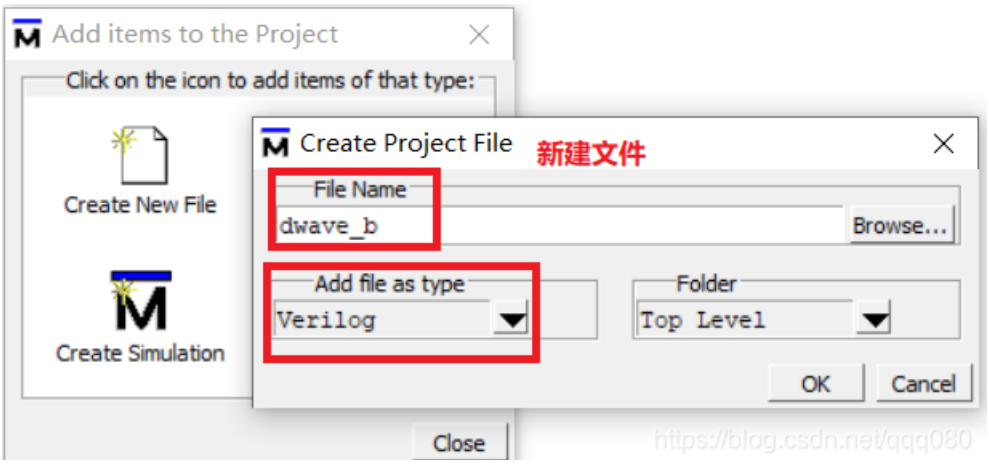
①添加现存文件
②创建新文件



将之前Quartus编译得到文件加入到工程里面。



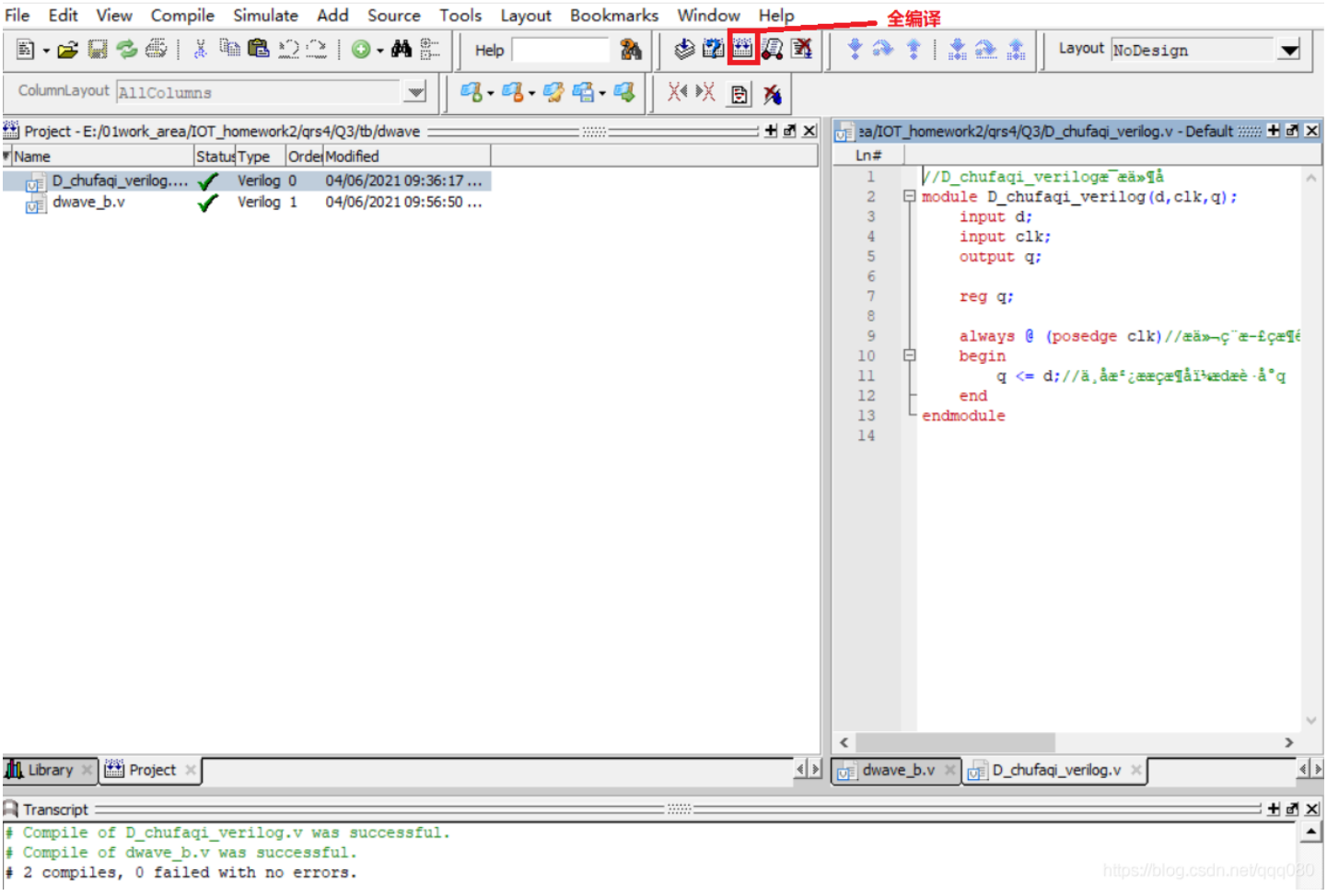
新建文件dwave_b.v



代码如下

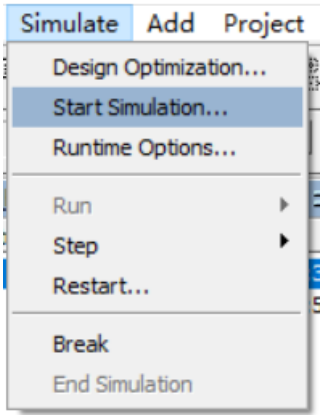
```
//测试代码
`timescale 1ns / 1ns

module dwave_tb;
    reg clk,d;
    wire q;

    dwave u1(.d(d),.clk(clk),.q(q));

    initial
    begin
        clk = 1;
        d <= 0;
        forever
        begin
            #60 d <= 1;//人为生成毛刺
            #22 d <= 0;
            #2  d <= 1;
            #2  d <= 0;
            #16 d <= 0;//维持16ns的低电平，然后让它做周期性的循环
        end
    end

    always #20 clk <= ~clk;//半周期为20ns,全周期为40ns的一个信号
endmodule
```

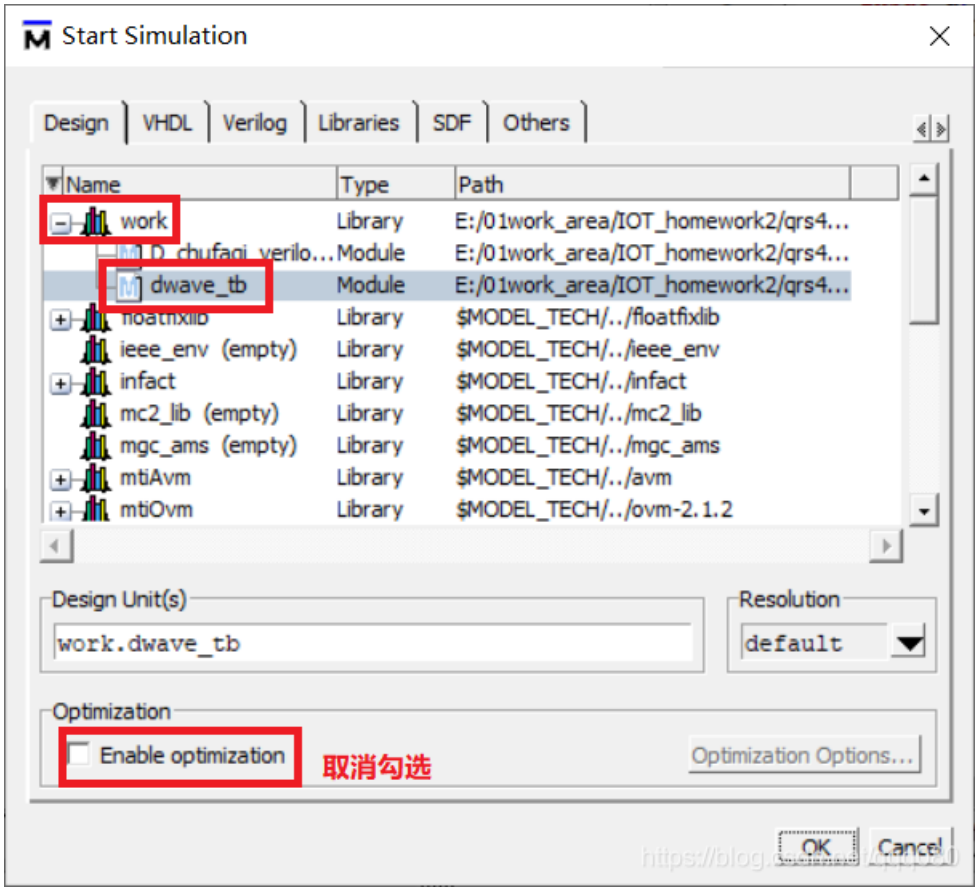
编译它们。



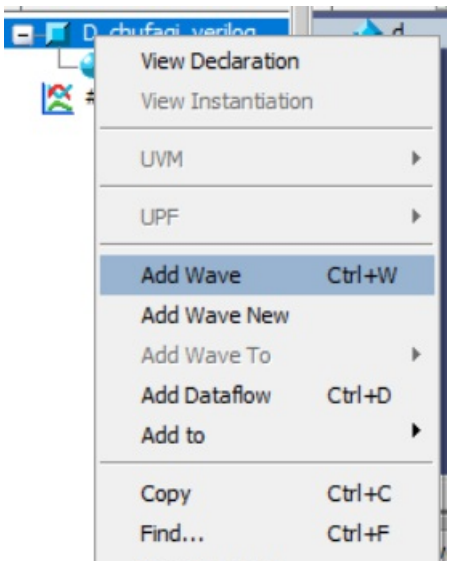
4.波形仿真

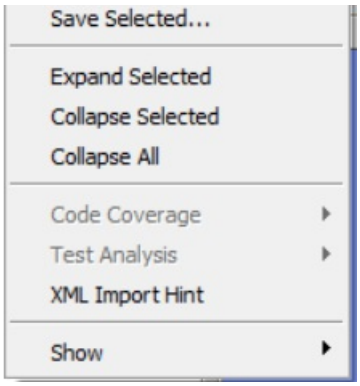
开始仿真



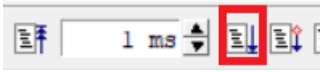


右键点击工程名，添加波形





设置好时间为1ms，点击旁边的按钮



会出现和上面差不多的波形。

我这出现了些错误，正在寻求解决

Error loading design